Design and implementation of reversible integer quaternionic paraunitary filter banks on adder-based distributed arithmetic

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Abstract: This paper presents a design method of reversible integer quaternionic paraunitary filter banks (Int-Q-PUFB) using the adder-based distributed arithmetic (DAΣ) for implementation multiplier block-lifting structure modules. The proposed quaternion multiplier (Q-MUL) and 8-channel Int-Q-PUFB processors are implemented on the FPGA Xilinx Zynq 7010. The total magnitude response of analysis-synthesis system based on the given Int-Q-PUFB shows that the 8-channel 8 × 24 Int-Q-PUFB is perfect reconstruction filter bank for finite precision. Compared to known solutions of Int-Q-PUFB using block-lifting

structure based on the CORDIC devices and ROM-based distributed arithmetic the given DAΣ-based Int-Q-PUFB have more less implementation complexity and latency.

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