Structurally orthogonal finite precision FPGA implementation of block-lifting-based quaternionic paraunitary filter banks for L2L image coding Nick A. Petrovsky 1, Eugene V. Rybenkov 2, Alexander A. Petrovsky 3

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Abstract: This paper presents a systematic design of the integer-tointeger invertible quaternionic multiplier based on the block-lifting structure and pipelined embedded processor of the given multiplier using distributed arithmetic (DA) as a block of M-band linear phase paraunitary filter banks (LP PUFB) based on the quaternionic algebra (Q-PUFB). A bank Q-PUFB based on the DA block-lifting structure reduces the number of rounding operations and has a regular layout, and can be implemented on the FPGA-based devices as integer-to-integer transform. Compared to general-purpose Q-PUFB obtained using lifting factorization, it needs less lifting steps and the given DA-based Q-PUFBs have less number of rounding operations and this property is useful for the lossless-to-lossy (L2L) image coding. Furthermore our DA-based 8-channel LP Q-PUFBs presented superior coding results on the PSNR than the corresponding filter banks, especially for image with relatively strong highpass components.

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