

# Optimal Low Power XOR Gate Decomposition

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**Abstract—This paper is dealing with power consumption of XOR based circuits. The bounds for switching activities have been obtained. The algorithm for XOR based circuits synthesis with minimal switching activity is offered.**

## I. INTRODUCTION

In the past, the major concerns of VLSI design were performance, area and reliability. However, this has begun to change recently, and power is being given comparable weight to speed and area. Two factors mainly contribute to this trend. On one hand is the remarkable success and growth of portable applications which demand high-speed computation and complex functionality with low power consumption. Without low-power design techniques, future portable devices will suffer from either a very short battery life or a very heavy battery pack [1]. On the other hand, power dissipation in high-end products rises with increased integration density and circuit speed. The resulting heat will increase the packaging and cooling costs and shorten the life of ICs. Therefore, low-power techniques are also needed.

In this work we considered a problem low-power decomposition of XOR based circuits.

## II. POWER ESTIMATION

In current technology, power dissipation in digital CMOS circuits is dominated by the dynamic dissipation, which is mainly the charging and discharging of the load capacitances [2]. In a circuit consisting of  $n$  gates, it can be modeled as

$$P = 0.5V_{dd}^2 f_{CLK} \sum_{i=1}^n C_L^i WSA_i, \quad (1)$$

where  $V_{dd}$  – is the supply voltage,  $f_{CLK}$  – is the clock frequency,  $C_L^i$  – is the load capacitance at the output of gate,  $WSA_i$  – is the expected number of transitions per clock cycle (referred to as switching activity),  $n$  – number of nodes.

We assume the zero delay models where gate delays are assumed to zero. Also we assume that load capacitance of every nodes is equal. We also assume that supply voltage and clock frequency is constant. Thus we must calculation switching activity for every node for estimation of power consumption circuits.

Most techniques are used signal probability for calculation switching activity of internal nodes [2]. Start from the primary inputs, for each gate  $z = x \oplus y$ , the probability  $p_z = p_x + p_y - 2p_x p_y$ . Then switching activity was calculation by:

$$WSA_i = 2p_i(1 - p_i), \quad (2)$$

where  $p_i$  – is the signal probability,  $i$  – is the number of the node.

This technique allows calculating average switching activity of node. But in practice most important know maximal value of switching activity. So we will be used technique from [3]. The main idea of this technique consists of different time for switching. So every input switching translates onto output (fig.1).

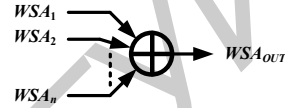


Fig.1. Multi input XOR element

In this case, switching activity of internal nodes was calculated by:

$$WSA_{OUT} = WSA_1 + WSA_2 + \dots + WSA_n. \quad (3)$$

Switching activity of input nodes was calculated by (2). Thus we can get maximal estimation of switching activity and used this estimation for XOR-based circuits design.

## III. GATE DECOMPOSITION

Technology decomposition is the step before technology mapping which decompose multiple-input logical elements into a network with only two-input gates (three, four, and all).

In [4] was described a problem of decomposition a multi-input XOR gate into a tree of two-input XOR gates. But technology library contain different primitives such as tree, four, eight input gates (as example, see [5]). In this work we consider decomposition multiple-input logical elements into a network with any input gates.

We assume:  $n$  – number of inputs multi-input logical element,  $d$  – number of inputs gate,  $k$  – number of gates. Under these assumptions, number of gates, which is needed for making  $n$ -input XOR on  $d$ -input gates, was calculated as:

$$k = \left\lceil \frac{n-d}{d-1} \right\rceil + 1, \quad (4)$$

where  $\lceil x \rceil$  – is nearest integer, greatest or equal  $x$ .

## IV. SWITCHING ACTIVITY ESTIMATION

As has shown in [4], exist many different variants of decomposition multi-input logical elements. This variant has equal number of gates but different switching activity. First we consider case of maximal switching activity. As shown in [1], maximal switching activity have signal with

probability 0,5. This signal is high-usage for testing of digital circuits [4]. According to [2], maximal switching activity is also 0,5. Example of maximal decomposition was presented on fig.2 ( $d=3$ ).

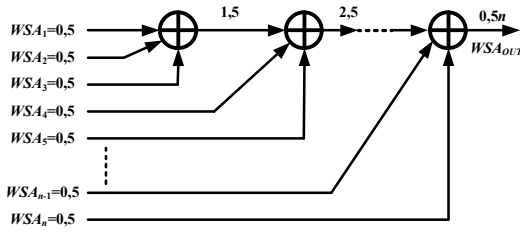


Fig.2. Example of decomposition  $n$ -input element on three-input  $XOR$  gates

So

$$WSA_{\max} = 0,5n + \sum_{i=1}^{k-1} (2i + 0,5), \quad (5)$$

where

$$k = \left\lceil \frac{n-3}{2} \right\rceil + 1. \quad (6)$$

Simplify (5), we get

$$WSA_{\max} = 0,5(n + k^2 - 1). \quad (7)$$

So

$$WSA_{\max} = 0,5n + \sum_{i=1}^{k-1} (2i + 0,5), \quad (8)$$

By induction we can calculate maximal switching activity for any  $d$ :

$$WSA_{\max} = 0,5n + \sum_{i=1}^{k-1} ((d-1)i + 0,5). \quad (9)$$

Based on results, was presented in [4], we can write expression for calculated minimal switching activity for any  $d$ :

$$WSA_{\min} = 0,5(n \cdot \lceil \log_d n \rceil + 2(n - 2^{\lfloor \log_d n \rfloor})). \quad (10)$$

## V. ALGORITHM FOR SYNTHESIS WITH MINIMAL SWITCHING ACTIVITY

For the synthesis of multi-input  $XOR$ -based circuits with minimal switching activity can be used the following recursive algorithm (assume that switching activity for any input is equal 0,5):

1. Find the switching activity of output:

$$WSA_{out} = 0,5n. \quad (11)$$

2. Imagine the switching activity of the output as the sum of the  $d$  numbers

$$WSA_{out} = WSA_1 + WSA_2 + \dots + WSA_d, \quad (12)$$

so that the following restrictions:

$$|WSA_i - WSA_j| = 0,5 \text{ or } |WSA_i - WSA_j| = 0, \quad (13)$$

where  $i \neq j$ ,  $i = \overline{1, d}$ ,  $j = \overline{1, d}$ .

3. If the value  $WSA_i$ ,  $i = \overline{1, d}$  is equal to  $x$ , then for him the algorithm ends, otherwise we apply step 2 to this value.

Consider this algorithm for  $n=10$ ,  $d=3$ .

1.  $WSA_{out} = 0,5 \cdot 10 = 5$ .

2.  $5 = WSA_1 + WSA_2 + WSA_3 = 1,5 + 1,5 + 2$ .

Restrictions (13) is true.

3. Check the value  $WSA_i$ ,  $i = \overline{1, 3}$  is equal to 0,5. It is false for all values, so we repeat step 2 for this values.

Example was show on fig.3.

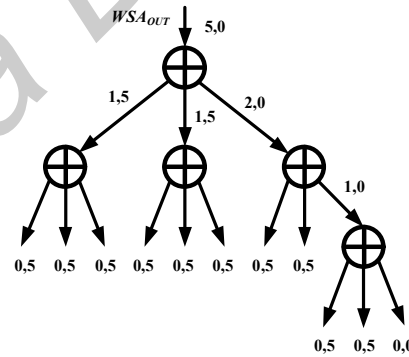


Fig.3. Example of decomposition 10-input element on three-input  $XOR$  gates with minimal switching activity

## VI. CONCLUSION

This work has touched on a problem of decomposition multi input  $XOR$ -based circuit. A estimation of switching activity (maximal and minimal) was finding. A algorithm for synthesis of multi-input  $XOR$ -based circuits with minimal switching activity was proposed. This algorithm can be used in computer-aided environment.

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