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THE IMPACT OF ESD ON MICROCONTROLLERS

Edited by PhD, Aassociate professor Viktor F. Alexeev

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Minsk
"Kolorgrad"
2018

UDC 004.31:621.382.049.77

The Impact of ESD on Microcontrollers / Gennady A. Piskun, Viktor F. Alexeev, Sergey M. Avakov, Vladimir E. Matyushkov, Dmitry S. Titko ; Edited by PhD, Aassociate professor Viktor F. Alexeev. – Minsk : Kolorgrad, 2018. – 184 p. – ISBN 978-985-7148-40-0.

Modern methods and means of testing the stability of microcontrollers to the effects of electrostatic discharges are considered. The analysis of functional and operational characteristics of microcontrollers with a program code written in the built-in flash memory is performed. A damage mechanisms classification to microcontrollers after the influence of electrostatic discharge and the possibility of developing new algorithms for technical diagnostics of microcontrollers are proposed.

On the basis of thermal processes analysis occurring in current-carrying elements of integrated circuits, the dependence of temperature, electric field strength and power of electromagnetic losses in each element and in their contact areas is shown, depending on the electrostatic discharge voltage. It is shown that electrostatic discharge affects change in programmed data in microcontrollers.

The method of functional control of microcontrollers, after exposure to static electricity discharges, developed by the authors is described; this method makes it possible to improve the result of culling of potentially unreliable products by obtaining information about possible violations in the built-in flash memory of microcircuits.

The monograph is intended for scientists, engineers, graduate students and undergraduates working in the field of integrated circuits reliability assessment. It can be used by senior courses students of relevant specialties.

Tables 32, figures 67, bibliography 174.

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ISBN 978-985-7148-40-0

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ACRONYMS

AE	– airborne equipment
BFM	– built-in flash memory
CDM	– charged device model
CM	– computer model
CMOS	– complementary metal-oxide-semiconductor
EM	– electronic mean
EMC	– electromagnetic compatibility
EME	– electromagnetic environment
EMI	– electromagnetic interference
EMP	– electromagnetic pulse
ESC	– electrostatic charge
ESD	– electrostatic discharge
FU	– functional unit
HBM	– human body model
IC	– integrated circuit
LSIC	– large-scale integration circuit
MC	– microcontroller
MPS	– microprocessor system
PC	– program code
RAM	– random-access memory
ROM	– read-only memory
SED	– static electricity discharge
SM	– simulation model
TC	– technical characteristics
TG	– test generator
TM	– test module
VLSIC	– very large-scale integration circuit

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PREFACE

Constant work on preservation and development of scientific, technological and innovation potentials is carried out in the Republic of Belarus. The system of science management is improving, the legal and regulatory framework of scientific and innovative activities is expanding and strengthening, measures are taken to increase the level of innovation production, to develop the infrastructure and companies, which are focused on new and innovative technologies [1].

Belarusian industry produces a variety of technical means, that include in their composition modern microelectronic products – microcontrollers, which perform management of electronic devices. Due to a variety of functional opportunities, their extensive range provides the developers with good conditions for designing complex hardware of various purposes. At the same time, it is quite difficult to implement effective protection of microcontrollers from external impacts, especially from such a destructive effect as electrostatic discharge.

Modern researches, presented in scientific and technical literature, provide the results, confirming the destructive impact of static electricity discharges on airborne equipment (AE) of spacecrafts [2–5], on-board digital computers [6], on objects of weaponry and military equipment [7, 8], on printed circuit assemblies of AE and electronic means [9–12], on mining and geological equipment [13, 14], on oil storage systems [15], on gas metering systems [16] etc. It is known that 8 to 33% of all injuries of electronic means and their components are caused by static electricity, that is the producer's annual loss of billions of dollars [17, p. 9].

In this connection, at the present moment there is a great number of publications in the field of determining the impact of static electricity discharges on the functionally complex products of solid-state electronics. The most significant results were obtained by Russian and Belarusian scientists, who conducted

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researches in such areas as the impact of static electricity discharges on semiconductor products (M. I. Gorlov, V. A. Emelyanov, L. P. Anufriev etc) [18–22]; methods of protection of devices from electromagnetic interference (L. N. Kechiev etc) [17, 23]; protection of integrated circuits from destructive pulses (V. A. Kaverznev, H. D. Hrosheva etc) [24–26]. Among the foreign authors, particular interest arouse the publications of C. Jowett [27], E. Habiger [28], A. Schwabb [29], A. Ameraseker [30], O. Semenov [31] and Steven H. Voldman [32, 33], which include descriptions of some mechanisms of impact and simplified analytical approaches for solving the problems associated with the impact of static electricity discharge on devices.

Using known methods of technical diagnostics of semiconductor devices is inappropriate in case of damage analysis of microcontrollers after accidental or intentional impact of electrostatic discharges. This is caused by the specifics of formation the semiconductor chip's architecture and the presence of such built-in functional unit as flash memory that stores the program code of any complexity. This feature significantly complicates the stability testing to the effects of static electricity discharge, since failures can occur not only as a result of damage of the chip elements, but also due to changes in the recorded data array, fault analysis of which is currently missing in the algorithms.

Taking into account the specifics of microcontrollers, based on performance of programmed functions, close attention should be paid to the security of information resource, as well as to the protection of the data from accidental or intentional damage. The problem of the protection of information is a multifaceted complex task, involving consideration of the security issues of the written into the built-in flash memory program code's integrity (protection from failures, leading to the loss of information, and protection from the loss of data) [34, p. 9].

However, the problem of controlling the functional and operational characteristics of microcontroller with the written into built-in flash memory program code after the impact of static electricity discharges is not fully developed.

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In particular, scientific and practical interest is the development of methods of functional and operational diagnostics of microcontrollers with the check of integrity of the recorded data array and the identification of areas of their unstable operating due to appeared changes in the code and other.

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CHAPTER 1

MODERN METHODS AND MEANS OF TESTING MICROCONTROLLERS RESISTANCE TO THE ELECTROSTATIC DISCHARGE

Microcontrollers of various purposes can be quite effective if they have high reliability, which is laid at the design stage, and is provided in the manufacture and exploitation. In this regard, one of the most urgent problems of modern electronics is the neccesity of systematical monitoring of the functional and performance characteristics of microcontrollers at all the stages of their life cycle.

This chapter provides an analysis of types and mechanisms of the impact of electrostatic discharges on microcontrollers, as well as a review of modern principles and means of testing on immunity to electrostatic discharge. This chapter also reviews the specificity of technical diagnostics of microcontrollers taking into account design and technological features, provides a classification of their damage and marks main requirements for conducting tests on resistance to the static electricity discharges. The necessity of the analysis of the program code, written into the flash memory of microcontrollers, after the impact of pulse discharges is proved.

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1.1. Analysis of types and mechanisms of impact of static discharge on microcontrollers

The appearance of electrostatic charges is often caused by the nature of static electrization, which covers all the processes leading to the formation and

separation of positive and negative electrical charges as a result of mechanical deformation, which occurs at a collision or contact of surfaces of two solids, surfaces of solid and liquid, as well as rupture or separation of surfaces of solids or liquids by gases or any other agent, in particular, ionized gases [1, p. 15–19; 2, p. 14]. These charges accumulate in a particular electrical capacitance and create an electric potential, which in some cases can be controlled by specialized technical means or special events. However, in most cases there is the occurence of ESD, which leads to the electromagnetic interference (in case of propagation of the discharge in gas) or to the uneven distribution of temperature gradients (in case of passing of the discharge pulse in the system of current-carrying elements).

Nowadays it is quite difficult to analyze all the ways of impact of static electricity discharges of microcontrollers. This happens because various kinds of impacts usually occur in complex, often one after one without visible boundaries between them.

Commonly the static electricity discharges can be characterized by two basic parameters: the type of discharge and the mechanism of impact.

1. According to [3–6] discharges are divided into the following types:

- contact discharge, which is used in the resistance tests of MC to the ESD, occurs when the discharge tip of the test generator is held in contact with the integrated circuit during the discharge;
- air discharge, the specificity of which is that during its implementation the tip of the test generator is gradually approaching to the integrated circuit till the electromagnetic pulse appears.

Testing MC for resistance to the contact discharge of static electricity is the most preferred, because air discharge is unpredictable and depends on many factors, leading to the changes in the pulse rise time and magnitude of the

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discharge current, for example, the approach speed of the discharge tip, ambient humidity and structure of the testing equipment.

2. During the analysis of [3–6] the main mechanisms of impact of ESD were identified, among which are the following:

- direct mechanism, i.e. static electricity discharges affect only those points and surfaces of MC, which are available for staff during normal exploitation;
- indirect mechanism, which simulates the impact of pulsed-contact discharges by delivering them from the test generator on the connection plates, while formed electromagnetic field leads to a malfunction of integrated circuits.

In the first case, there is a direct injection of charge in the system of current-carrying elements of MC, and in the second – effects are related to the radiated electromagnetic interferences and therefore are indirect.

1.2. The principles and means of testing microcontrollers resistance to electrostatic discharge

During the monitoring of functional and operational characteristics of microcontrollers caused by the impact of static electricity discharges close attention is paid to two types of failures that differ in the nature of malfunction [7]:

- parametric failure of the microcontroller, after which microcontroller preserves its functioning, but values of one or more parameters go beyond the limits, that are set in the normative or technical documentation;
- functional failure of the microcontroller, that causes the termination of its functioning, which is not provided by regulated conditions.

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In this connection, two types of tests are conducted with the subsequent processing of the results:

- parametric testing, during which the electrical (static and dynamic) characteristics are checked to be in the limits, that are provided by technical conditions [8, p. 157–218];
- functional testing, which is based on monitoring realized by the microcontroller's programmed functions, that are defined by their manufacturer [8, p. 219–230].

Taking into account that the number of methods of parametric and functional testing on modern manufactures of semiconductor industry is quite diverse, we are going to consider the basic requirements for the testing of microcontrollers given electrical and functional parameters.

1.2.1. Requirements for testing taking in account analysis of electrical parameters

There are three main sources, which accumulate static electricity because of production and exploitation of microcontrollers, and which are the cause of their failure due to the occurrence of discharge:

- human, charged with static electricity, touches the product and discharges to it and then through it to the ground;
- the product itself, playing the role of one of the capacitor plates and accumulating an electrostatic charge, its contact with the grounded object can cause a discharge of static electricity and the subsequent failure of the device;
- the electric field generated by charged objects; under certain conditions, a product, placed in such a field, may acquire a significant potential difference between the opposite surfaces, which would cause the discharge.

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Considering the above, modern manufacturers of MC use specialized equipment that simulates the impact of static electricity discharges during the testing of developed products for resistance to ESD. This equipment, which includes generators of charge, is built on three basic models of pulsed discharge: human body model, HBM [3–6; 9, p. 18–27; 10, p. 24–26; 11, p. 29–30; 12–16]; machine model, MM [6; 9, p. 27–28; 10, p. 26–27; 11, p. 30; 17–21] and charged device model, CDM [9, p. 28–40; 10, p. 28–30; 11, p. 30; 22–25].

The most studied and widespread testing model of resistance of MC to ESD is the human body model. This mainly comes from the fact that, as well as the machine model, it is designed to simulate the discharge from the charged object (human or machine) during its direct contact.

Let us consider the basic principles of the resistance testing of microcontrollers to the impact of static electricity discharge on models mentioned above.

1. Requirements to the resistance testing of microcontrollers to static electricity discharge on the human body model.

One of the most common objects of electrization is a human (operator), who accumulates static electricity charge up to fifteen kilovolts, which may cause damage to microcontroller.

This charge is generated on the human body basing on the following physical mechanisms [1, p. 15–19; 2, p. 15–17]:

a) triboelectric – during the contact and separation of two objects one of them is always charged positively and the other is charged negatively.

b) inductive – when moving charged objects close to uncharged, in the latter static charge with the opposite sign is generated and, as a consequence, an induction current appears.

c) capacitive – the charge is the voltage multiplied by the capacitance, so, when the value of charge is constant, capacitance reduction leads to the growth of potentials of separated surfaces.

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With relatively simple movements on the surface of the human body significant electrostatic charge can be created (table 1.1) [26; 27].

Table 1.1. The voltage of electrostatic discharge, appearing during various operations [26; 27]

Operation	Voltage of ESD at a relative humidity, kV		
	10%	40%	55%
Walking on the carpet	35	15	7.5
Walking on the floor covered with vinyl	12	5	3
Movement on the bench	6	0.8	0.4
Withdrawal of MC from the plastic canister	2	0.7	0.4
Removing MC from the vinyl plate or tray	11.5	4	2
Withdrawal of MC from the plastic package	14.5	5	3.5

It should be noted that in the description of the impact of ESD using HBM some assumptions were made. First of all, the model represents rather simplified distributed system (the human body), and it does not take into account corona phenomenons, which appear just before the discharge. Also it does not take into consideration the inductance value of human body 50–100 μH, which in some extent limits the edge steepness of ESD. Besides, the observed discharge of this type takes place not once, but as a series of successive discharges at lower voltages.

This model, for example, often occurs when a charge carrier (human) touches contact pins of MC in case of manual assembly operation (figure 1.1), and part of energy, which is contained at the surface of his body, is transmitted, i.e discharges to the MC and through it to the ground [1, 3].

It is quite difficult to reproduce the complete model of the discharge from human body on practice, so native and the majority of foreign standards provide

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only superficial RC-components and the maximum rise time of pulse of 20 ns (figure 1.2) [1, p. 262, figure 6.4; 9, p. 20, figure 3.3; 10, p. 25, figure 2–3; 3–6].

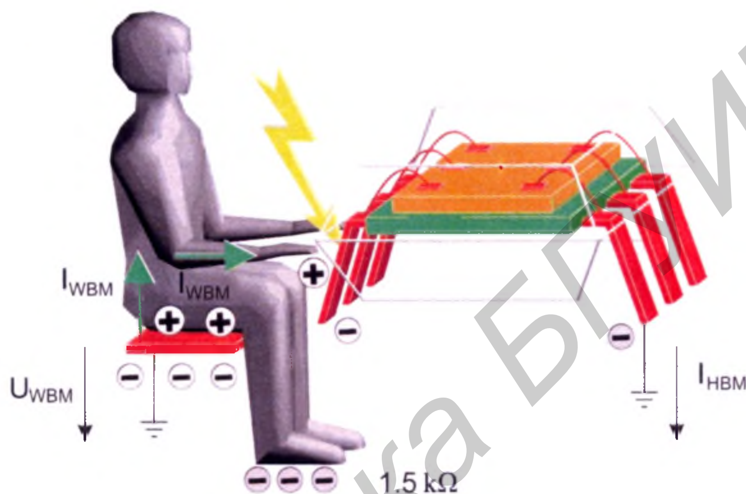

Figure 1.1. The impact of ESD on external pins of the microcontroller on the human body model [1, 3]

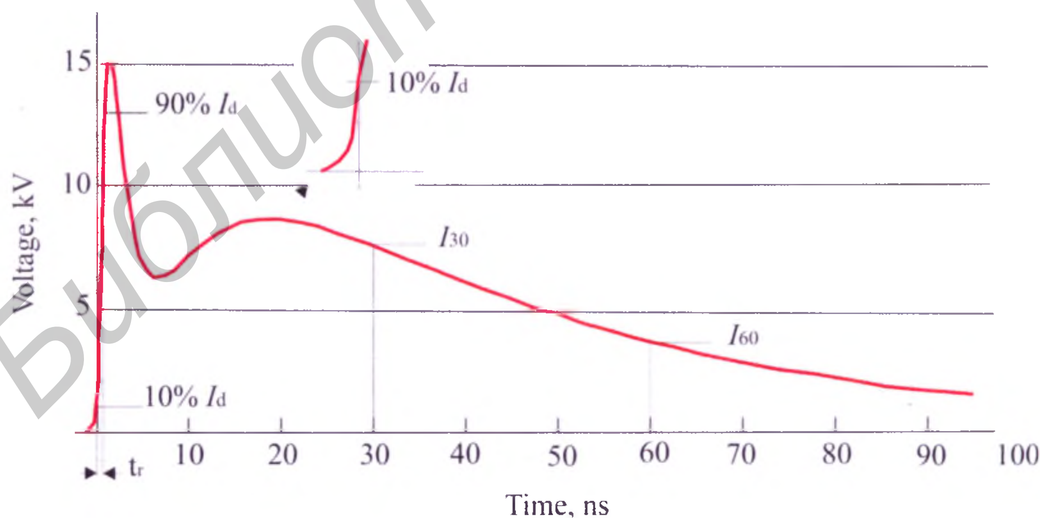

Figure 1.2. Graphic of the dependence of discharge current on time, received from the test generator, simulating the discharge of static electricity from the human body

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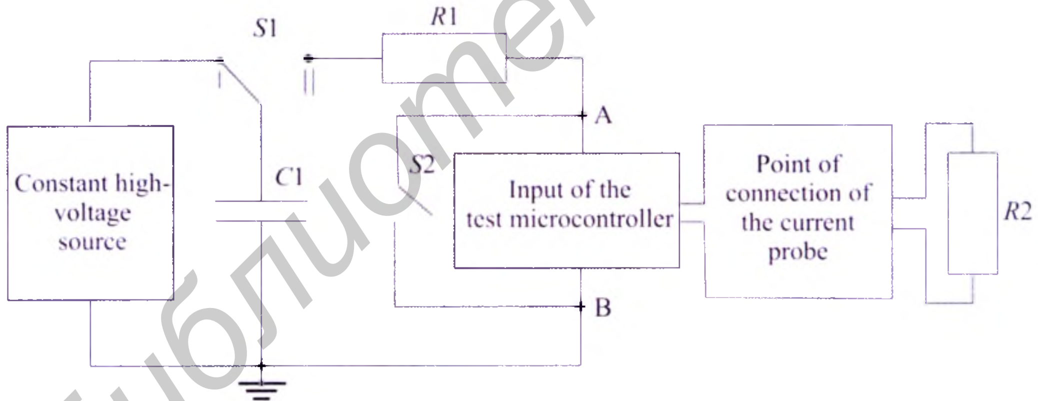
The equivalent circuit of the test generator that simulates the impact of the discharge on HBM, generally consists of connected in series capacitance and resistance. STB IEC61000–4–2–2006 [3] is a current standard on the territory of the Republic of Belarus in the field of testing of resistance to electrostatic discharges. Capacitance and resistance of the human body (the operator) in this standard equal to values C_{HBM} = 100–2500 pF and R_{HBM} = 80–2000 Ω, which corresponds to a standing separately human carrying a charge on the entire surface of the skin. Average level of charge accumulated on the human body is 12 kV with the charge energy equal to the 15 mJ, at the maximum voltage of 15 kV the charge energy is 17 mJ. When testing on HBM, test generators have the following structure (figure 1.3) [1, p. 272, figure 6.8; 28, p. 20, figure 10; 9, p. 19, figure 3.2; 10, p. 24, figure 2–2; 3–9].



R1 = (330 ± 1) Ω; R2 – non-inductive resistor with a nominal value (500 ± 1) Ω, rated at voltage of 4 kV; C1 – capacitor with capacitance (100 ± 10) pF

Figure 1.3. Scheme of the test generator that simulates discharge of static electricity from the human body

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Result of any single test situation can be used to compare threshold voltage of destruction levels of different MC. Levels, that are set in that way, have values typical for the worst case, because in most cases real discharge pulses with certain potentials are less than in test generators.

One of the most important parameters in the HBM is the current rise during the discharge. It is usually a few tenths of nanoseconds. It is important to note that the current of discharge does not spread immediately in the conducting field or in the system of current-carrying elements of MC. Therefore, in the beginning, there is a danger of an overload of protection circuit and then – the destruction of elements.

This model, for example, often occurs when a charge carrier (human) touches the external pins of microcontroller in the case of manual assembly operation and part of the energy, which is contained at the surface of the body, is transmitted, i.e. discharges to the integrated circuit and through it to the ground.

2. Requirements for testing of microcontrollers resistance to static electricity discharge on the machine model.

A distinctive feature of MM compared with HBM is that in MM another charged device or machine carries ESD. The charge, accumulated on the metal parts of substrate and housing, flows through the substrate and causes failures of p-n junction, dielectric layers and elements.

An example of the case, described by the machine model, can be observed during automatic feeding of microcontrollers by sliding in the supply channels (figure 1.4) [21]. The system of external pins of MC and its housing can be charged with static electricity as a result of friction, in the same way as the human body is charged during the operations connected with the process of friction [1, 21].

In contrast to the discussed above human body model, during the static electricity discharge on the machine model in the equivalent scheme there are only the values of self-capacitance of the object and its discharge resistance (figure 1.5) [1, p. 274, figure 6.9; 10, p. 27, figure 2–4].

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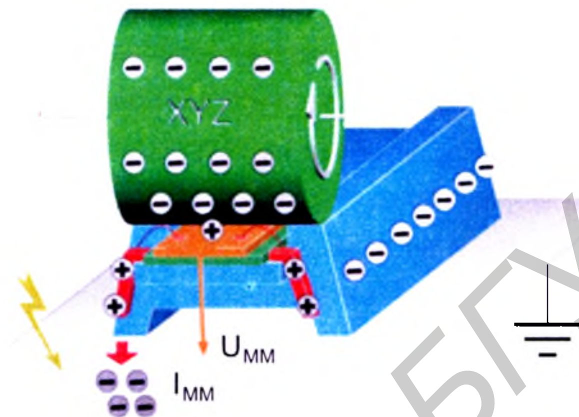
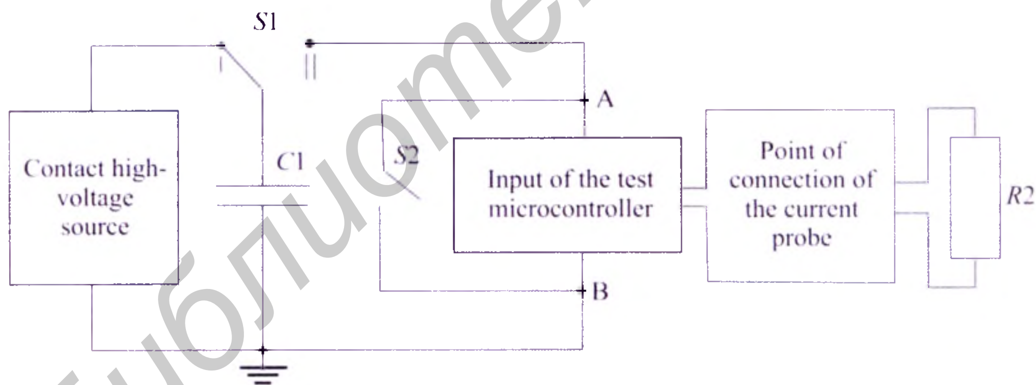


Figure 1.4. The impact of electrostatic discharge on the external pins of microcontroller on machine model]



R2 – non-inductive resistor with a nominal value (500 ± 1) Ω, rated at voltage of 4 kV; C1 – capatitor with capacitance (100 ± 10) pF

Figure 1.5 Scheme of the test generator that simulates discharge of static electricity from the charged device or machine

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Due to the small discharge resistance, the shape of the static electricity discharge pulse (figure 1.6) is determined only by the values of the parasitic elements of circuit of the test generator, that simulates the impact on microcontrollers [10, p. 27, figure 2–5].

An example of a case described by MM, can be observed in the automatic feed of MC by moving on assembly line. The system of its external pins and housing can be charged with static electricity by friction, in the same way as the human body is charged during operations connected with the process of friction.

Repeatability of the results of tests conducted using the machine model is much lower than using the human body model.

The main cause of damage of microcontrollers during the impact of ESD in MM is that the discharge pulse occurs so quickly that the dissipated power exceeds the damage threshold.

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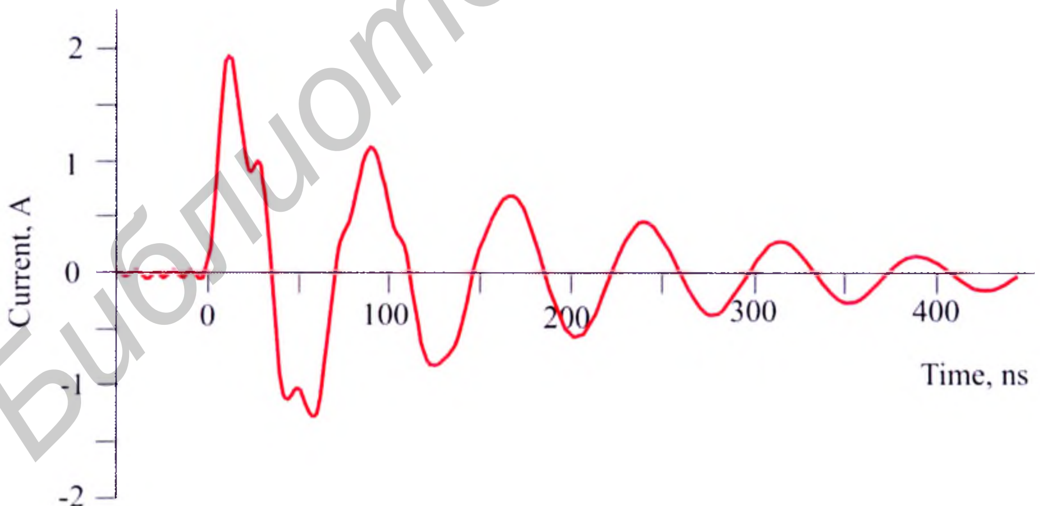

Figure 1.6. The graphic of dependence of discharge current on time, received from the test generator, simulating the discharge of static electricity from the charged device

3. Requirements for testing of microcontrollers resistance to static electricity discharge on the charged device model.

The model of this type considers a case when MC receives ESC during the manufacturing process, and then discharges to object, which has high conductivity (e.g., ground) (figure 1.7) [1, 21].

This extremely fast discharge does not lead to overheating of the defense circuit of MC from ESD (as it happens while using the HBM and MM), but it often leads to such breach in the structure of the MC as the breakdown of the insulating oxide layer [21].

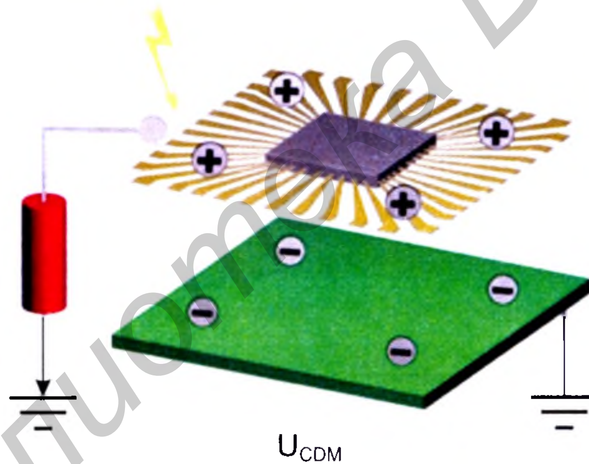

Figure 1.7. The impact of electrostatic discharge on the charged device model [1, 21]

The typical form of the discharge pulse during the test of MC for the resistance to ESD on CDM is shown on figure 1.8 [10, p. 29, figure 2–7]. His rising edge is much shorter (rise time is about 300 ps) and the total duration of pulse is significantly lower (about 0,5 ns) than the corresponding pulse parameters in HBM and MM. That means that the amplitude of the current in pulse reaches a few amperes even at low discharge voltages. When using the CDM, the level of power dissipated in the device is lower than with the HBM and MM [1].

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The rising edge is much shorter (rise time is about 300 ps) and the total duration of pulse is significantly lower (about 0,5 ns) than the corresponding pulse parameters in HBM and MM. That means that the amplitude of the current in pulse reaches a few amperes even at low discharge voltages. When using the CDM, level of power dissipated in the device is lower than with the HBM and MM.

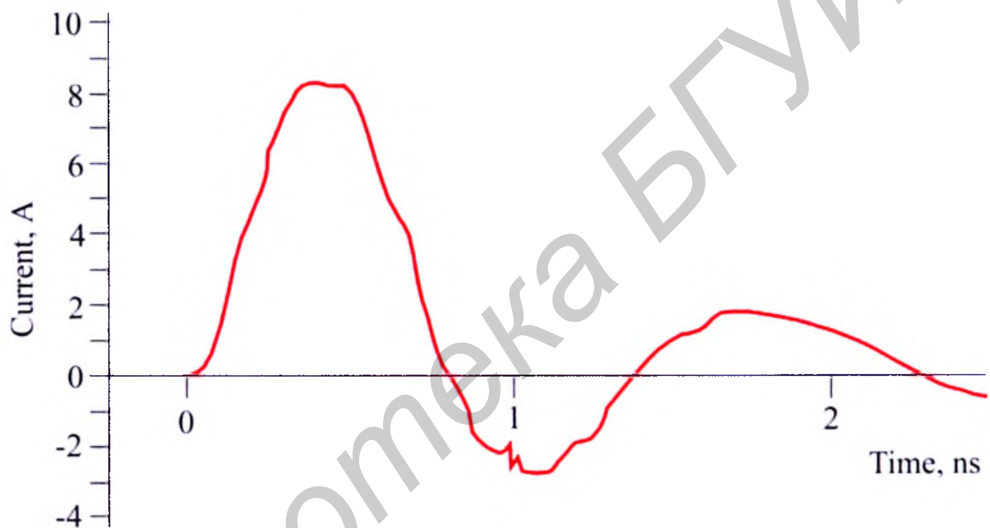

Figure 1.8. The graphic of dependence of discharge current on time, received from the test generator, simulating the discharge of static electricity from the object with a high conductivity

During the tests of microcontrollers resistance to the impact of ESD on CDM, microcontroller is removed from the panel and placed on a metal plate external pins up. First, the integrated circuit is charged by applying a charge on the «ground» pin through a high-value resistor or from a charged substrate by electrostatic induction. Then, external pins alternately discharge (by touching them with a grounded needle). As can be seen from the figure 1.9 [10, p. 28, figure 2–6], the chip of MC and a metal plate, on which the integrated circuit is placed, form a kind of capacitor. It's capacity depends on the geometry of the microcontroller's

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housing. The value of this capacity determines the value of the electric charge and current discharge amplitude. Since the discharge process begins with the appearance of a spark between the tested external pin of microcontroller and grounded needle, the repeatability of CDM test is not high.

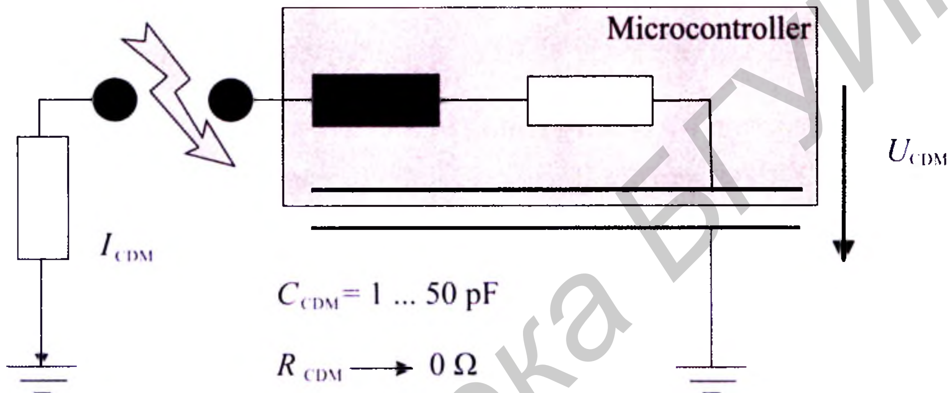

Figure 1.9. Scheme of a facility for simulating the static electricity discharge from a charged device

This facility simulates real situations, which arise during various manipulations with MC, very well. However, this extremely fast discharge does not lead to the overheating of the MC's circuit of defense from ESD (as it happens during the tests using HBM and MM), but it often leads to such breach in the structure of the MC as the breakdown of the insulating oxide layer.

All represented models are only an approximation of real situations. In fact, parasitic capacitive and inductive coupling can significantly reduce the fidelity of the model. The influence of parasitic coupling is the greatest in CDM.

Testing MC for resistance to ESD on the aforementioned models includes the following operations [29]:

– control of static parameters, which is a measurement of electrical quantities (input or output currents and voltages) in an established regime;

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– control of dynamic parameters, in which the measurements of timing of input and output of MC's signals are carried out, and time interactions of signals within the circuit is studied.

Control of static and dynamic parameters of MC in the production is performed by using special equipment.

1.2.2. Requirements for testing taking in account analysis of functional characteristics

When checking the functional characteristics of microcontrollers in the workflow, we can use the method of comparison the output parameters of the model with its standard version, connected in parallel with the test MC [8, p. 225; 6, 7, 12].

As informational parameters of diagnostic are often chosen the following ones: the heterogeneity of array of program code, the charge in the transition process at the moment of changing the information during writing or reading, time of completion of the transition process at the moment of the input impact and final current reaction to this impact [8, p. 225].

Block scheme of the test stand, which implements information and energy method of control, is shown on figure 1.10 [8, p. 225, figure 8.3].

The working principle of the device is the following. From the «unit of setting the impact» appropriate signals (running «0» or running «1») are transfered to the inputs of reference and test microcontrollers, output signals of which are substracted by «sunstraction unit». The difference between standard signal and test microcontroller signal is subjected to further processing. The obtained difference of signals is converted into a voltage by «converter current – voltage» block and then processing operation is performed by «integrator», from which the result of integration is rewritten into the «analog storage device» and it is

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controlled by «comparator» with defined boundaries of comparison, values of which are programmed. The results of comparison are processed by «result and control unit» using the principle «fit – reject» [8, p. 225].

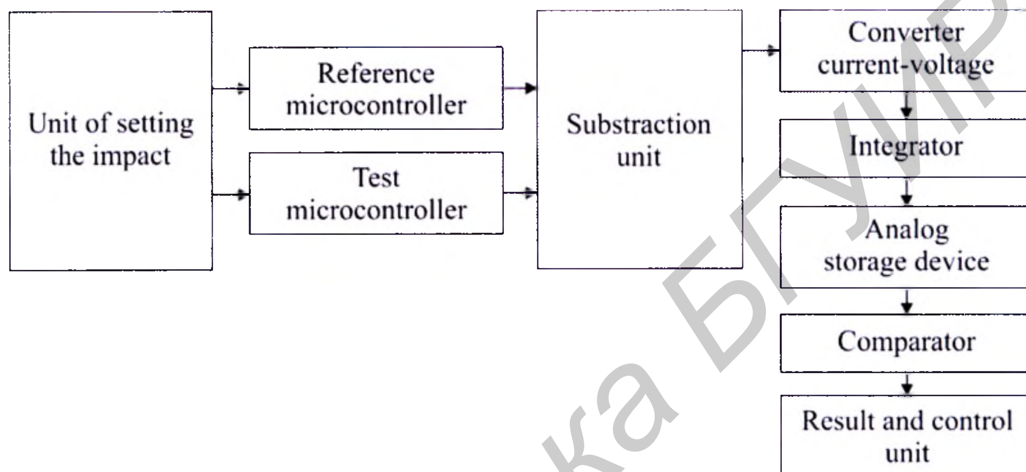

Figure 1.10. Block scheme of the stand, which implements information and energy method of control of microcontroller

The disadvantage of this method is the lack of information about the degree of deviation of code quality index (changes in the recorded data array), which can lead to false activation of MC.

The diagnostic methods of semiconductor devices are listed in [30–32], where control of inhomogeneity of any kind is in seeking of maximum deflection of controlled static time and charge parameters from value in the selected calibration array, in measurement of value of this deflection and fixating the cell address, in which this maximum deflection occurred.

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1.3. Technical diagnostics of microcontrollers after exposure to electrostatic discharge in accordance with their design and technology features

Microcontrollers are a class of microprocessor devices, that are focused on the performance of management functions of different objects [33, p. 19; 34, p. 8]. Due to the wide range of problems, which are solved by modern devices, the requirements for the main characteristics of this type of integrated circuits are quite diverse. However, it is possible to achieve the optimum in selection of a microcontroller only when internal structure and architecture of the processor core are known.

1.3.1. Organization of the internal structure

Microcontroller is a particular type of microprocessor electronics. Unlike microprocessors, which are only part of a microprocessor system, a single chip of MC includes microprocessor, ROM, RAM, serial and parallel input-output ports and ADC. One chip can not fully replace the microprocessor system, which is based on modern microprocessors, as it has less ROM, RAM and the bitness is much lower. However, for many purposes of control and management of various processes MC's capability is quite sufficient, so they are widely applicable among the developers of modern radioelectronic equipment [35, p. 284–286].

The structure of microcontroller determines the composition and interaction of main functional blocks, placed on its chip [35, p. 9].

The analysis of [35–38] revealed that the main feature of structure of MC is the placement of internal memory and a large set of peripherals with central processor in one chip. The composition of peripheral devices usually includes multiple eight-bit parallel input-output ports, one or two serial ports, timer unit, analog-digital converter. Moreover, various types of MC consist of additional

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specialized devices, which include the unit of forming signals with pulse width modulation, display controller and many others (figure 1.11) [39, p. 5, figure 1.1].

Figure 1.11 shows that modern MC are based on standard functional units, which include [35, p. 9; 39, p. 6–7; 40, p. 239–240]:

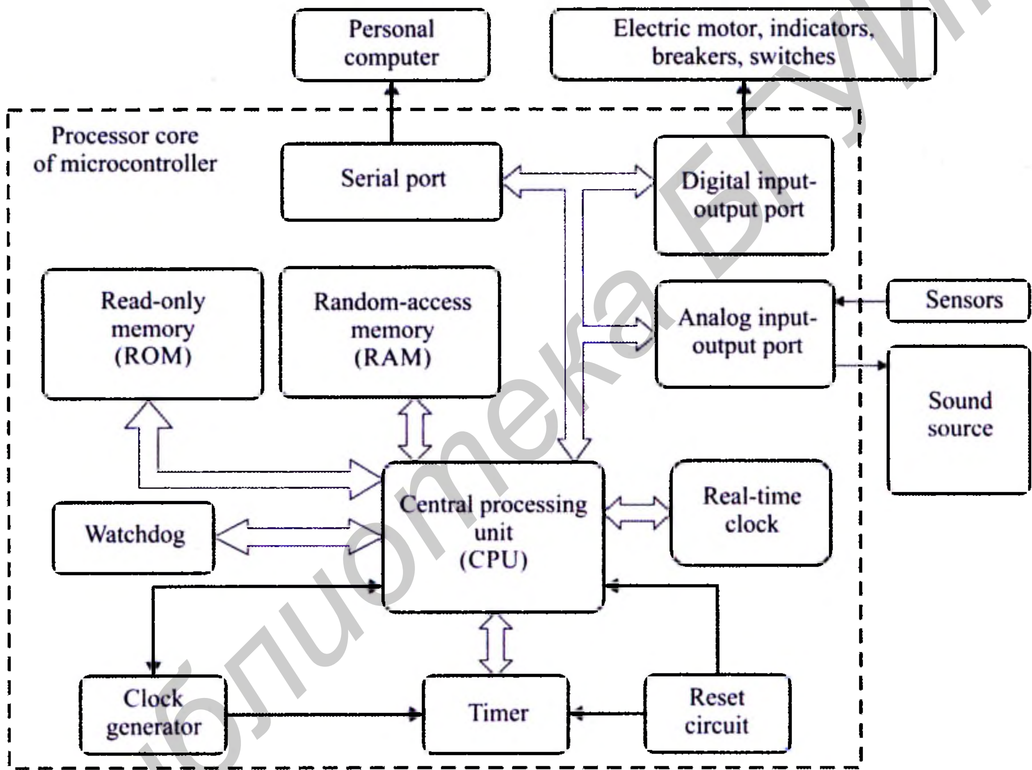

Figure 1.11. Scheme of interaction of MC with execution units

1. Central processing unit receives (CPU) instruction codes from the program memory, decodes them and executes. It includes an arithmetic logic unit (ALU), registers and the control circuits.

2. Read-only memory (ROM) is intended for storage of constant data arrays or rarely changed ones.

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3. Random access memory (RAM) provides the storage of temporary program code.

4. Clock generator initiates the operation of controller and determines the speed of microprocessor.

5. Reset circuit sets microcontroller to its original state that determines correct start of MC work.

6. Serial port allows exchanging data with external devices with a small number of wires.

7. Digital input-output port is required for simultaneous control of several external devices, addressing them between functional units with built-in lines.

8. Timer sets time intervals.

9. Watchdog timer is designed to prevent system failures of program, because after running the program it starts counting a predetermined time interval.

Specificity of modern microcontrollers, which include more sophisticated functional units (the increase of amount of RAM and ROM, time of processing information, etc.), as well as their extensive range, caused by a variety of functional capabilities, allows the developers of electronic products to design and produce complex competitive equipment for various purposes.

1.3.2. Organization of processor core architecture

It is quite difficult to imagine modern microelectronics without such an important component as microcontrollers. The reason for this is that devices, assembled on their base, become easier, do not require adjustments and have smaller overall dimensions. In addition, using of MC gives wide opportunities for enhancing consumer functions of device, that is achieved by quite simple reprogramming. Thus, in the course of long-term development of electronics, differentiation of microcontrollers by functional and structure features of the processor core architecture occured.

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The architecture of microcontrollers' processor is a complex of hardware and software means, which are provided to a potential user [35, p. 31; 36, p. 10].

To meet the demands of consumers a big range of 8-, 16-, and 32-bit MC is produced. All of them have processor core, which has the following architectures [41–45]:

– CISC (Complex Instruction Set Computer) – the architecture is implemented in many types of microcontrollers that perform a wide variety of comands using multiple adressing modes. A variety of commands and addressing modes allows a programmer to implement most efficient algorithms for solving various problems. However, this significantly complicates the structure of MC, especially its control unit, which leads to the increase of size and cost of a semiconductor chip, and the decrease of performance [35, p. 10];
– RISC (Reduced Instruction Set Computer) – microcontroller's architecture, that differs by using a limited instruction set of fixed format, as well as significant reduction of number of used adressing modes. The advantage of RISC-processors is that their simplified commands need less machine cycles, thereby increasing the productivity of MC [35, p. 10].

Apart from the set of commands and ways of addressing, an important architectural feature of MC is a type of memory implementation and organization of command data retrieval. Due to these features, processors are divided into processors with Princeton and Harvard architecture [45, p. 10–14].

Princeton architecture, which is often called the von Neumann architecture, is characterized by using common random-access memory for storing programs, data and for the organization of the stack. A system bus, by which the processor receives both commands and data, is used to access memory (figure 1.12) [45, p. 11, figure 1.6, a].

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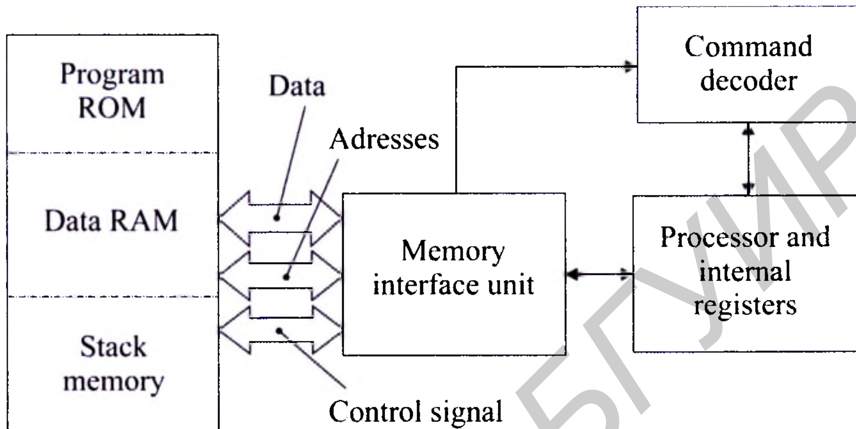

Figure 1.12. Architecture of a computing system with the Princeton architecture

This architecture has a number of important advantages. The presence of shared memory allows quick redeploying of its capacity for storage of particular data arrays, data and for stack implementation, depending on the task. Thus, it is possible to make better the usage of available random-access memory for each application of microcontroller. Using shared bus for transferring commands and data greatly simplifies debugging and testing of the system, increases its reliability. However, it has some significant disadvantages, the main one is the need for a consistent transfer of command and processed data retrieval by the common system bus. At the same time, it is necessary to make several requests to perform command retrieval.

Harvard architecture is characterized by the physical separation of command (program) memory and data memory. Each memory is coupled to the processor with a separate bus. That allows to make the next retrieval and to decode the next command simultaneously with reading/writing of data during the performance of current command. Block diagram of this architecture is shown on figure 1.13 [45, p. 11, figure 1.6, b]. Due to this solution, which is often used in modern functionally complex microcomponents, the most optimal and high performance is provided.

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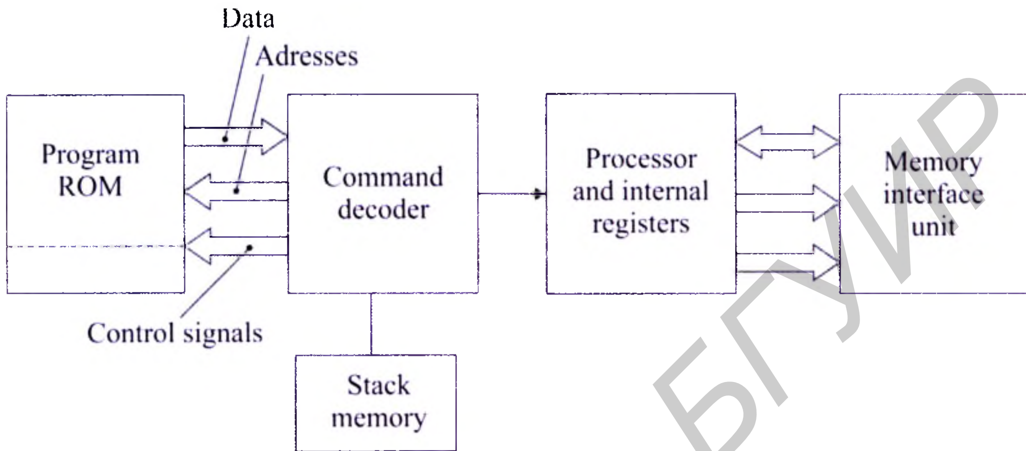

Figure 1.13. Architecture of computing system with Harvard architecture

Disadvantages of Harvard architecture include the need for more buses, as well as fixed capacity of memory allocated for commands and data, the purpose of which can not be quickly redeployed in accordance with requirements of the problem, which is being solved.

Due to the wide range of tasks of management of various objects, requirements for a modern MC are very diverse. In this regard, a large range of microcontrollers, which are usually divided into 8-, 16- and 32-bit, is produced to meet the needs of consumers.

Modern 8-bit MC represent the most numerous group of devices, which have a relatively low performance, but sufficient enough for a wide range of problems. They are simple and cheap, oriented on usage in quite simple devices of mass production (household and industrial systems, TV, video and audio equipment, communication means, etc.) [45, p. 37–54].

These processors are characterized by construction of the processor on the Harvard architecture, which uses separate memory for storing programs and data. For storage of manufacturers programs a mask-programmable ROM, once

programmable ROM or electrically erasable programmable ROM (such as flash memory) are commonly used. Internal program memory typically has a volume from several to tens of KB. If necessary, a number of MC allows you to connect an additional external memory for commands and date up to 64–256 KB.

The following families of 8-bit MC are used most widely today:

– family with processor core MCS-51 (Intel, Atmel, etc.) [46];
– family with processor core AVR (Atmel) [46];
– family with processor core PIC (Microchip Technology) [47].

Each of these families has its own features, which determine specificity of their usage for application problems.

Today a number of companies that have modified processor core produces MC with the base architecture MCS-51, developed by Intel. Because of this upgrade, performance was significantly improved (in MC produced by Winbond [48], NXP Semiconductors [49] commands are executed for 1–4 cycles instead of 12), the amount of program memory (up to 128 KB) and data (up to 2 KB) increased. Wide application in measuring and control systems found MC of company Analog Devices [50], in which the processor core MCS-51 is integrated with 12- or 16-bit analog-to-digital and 12-bit digital to analog converters.

The processor core AVR, used in the MC of Atmel company, is built with RISC-architecture, which allows to perform most of commands per one clock cycle, it provides higher performance comparing with the MC with CISC-architecture (MCS-51 and CPU08). Microcontrollers with AVR core contain a wide range of peripheral modules, have high performance and in recent years they are used more often then their analogues [46].

Microcontrollers with a processor core PIC (families of PIC12, PIC16 and PIC18) of company Microchip Technology also have RISC-architecture, which enables to perform commands per smaller number of clock cycles. At the same time, they

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have lower power consumption. Microcontrollers PIC12 and PIC16 implement the limited set of commands (less than 40); amount of internal data memory is rather small. Family PIC18 has more opportunities, it implements a number of additional commands and its volume of internal data memory is increased to 1 KB [47].

Main technical characteristics of modern MC of foreign production are presented in table A.1 (Appendix A).

Modern 16-bit MC in many cases are just improved modifications of their 8-bit prototypes. They are characterized not only by the increase of bitness of processed data, but also by the developed system of commands and addressing modes, increased number of registers and amount of addressable memory, as well as a number of other additional features, the use of which increases performance and provides new areas of use. The main area of application – complex industrial automatics, medical measuring equipment, communication equipment [43, p. 55–80].

The main producers of 16-bit microcontrollers are Infineon (family C16x) [51], Freescale Semiconductor (family HCS12) [52], STMicroelectronics (family ST10x) [53], Intel (family MCS-96/196) [46], Texas Instruments (family MSP430) [54], and also Japanese companies Renesas Technology, Fujitsu, Hitachi.

The main technical characteristics of 16-bit microcontrollers of foreign production are presented in table A.2 (Appendix A).

Modern 32-bit MC, which are used nowadays, contain high-performance processor, which is appropriate by its capabilities to the younger model of general-purpose microprocessors. In some cases, the processor used in these MC is similar to CISC- or RISC-processor, which are produced or used to be produced earlier as general-purpose microprocessors. Different models of computers and systems of management application and system software were created on the basis of these processors.

Technical characteristics of the most widely used 32-bit microcontrollers of foreign production are presented in table A.3 (Appendix A).

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1.3.3. Principle of formation of program data in the built-in flash memory of microcontrollers

As a resut of analysis of [36, 55] we can divide the structures of building of flash memory of microcontrollers into two main: a memory based on cells NotOR [36, p. 15, figure 17] and «NotAND» (figure 1.14) [55, p. 15, figure 18].

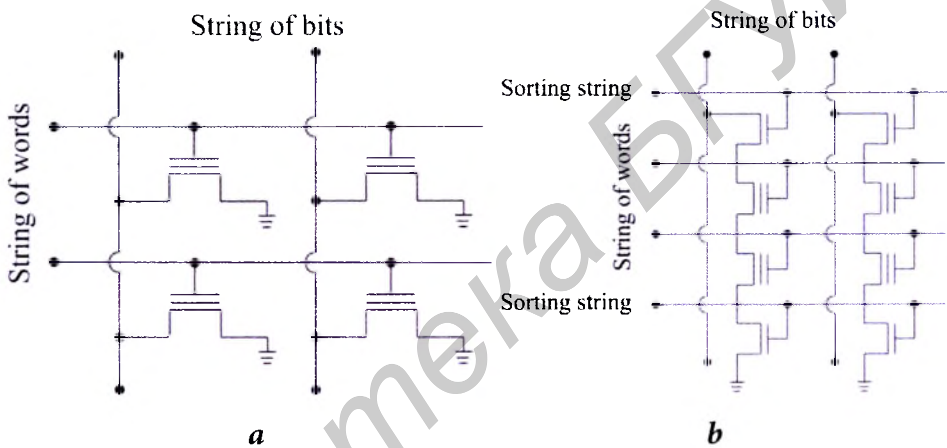

Figure 1.14. Structure of building of flash memory based on cells «NotOR» (a) and «NotAND» (b)

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The structure of cells «NotAND» consists of parallel-connected unit cells for storing information, organization of which provides the possibility of a random access to data and for a byte-serial entry of information. This recording is carried out by the injection of «hot» electrons; erasing is the result of the tunnel effect [56–58].

The basis of cell structure «NotOR» is the principle of serial connection of unit cells, forming groups of 16 cells, which are combined into pages and pages into blocks. In this arrangement of array memory, addressing to the individual cell is impossible. Programming is carried out only within a single page at a voltage of source, drain and substrate equal to 0 V and a gate voltage equals to 20 V. During erasure addressing is carried out to blocks and groups of blocks at

a voltage of source, drain and substrate equal to 20 V, and a gate voltage equals to 0 V, due to the tunnel effect [59–61].

Taking into account that cells «NotAND» and «NotOR» of flash memory of modern microcontrollers differ in their organization, they have one common element – transistor with a «floating» gate, which can be presented as in [62]. It is worth noting that this kind of MOSFET can store binary information for a long period.

This term originated from the fact that the potential of this area is not stable, that allows to accumulate electrons in it.

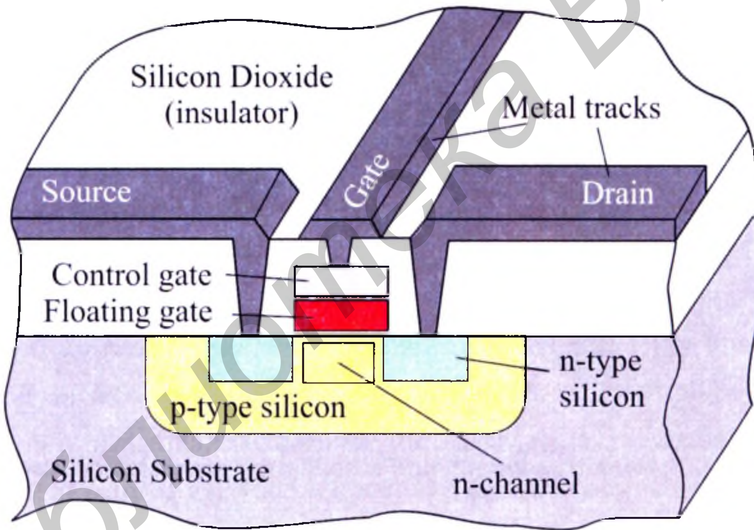

Figure 1.15. Schematic representation of transistor with a «floating» gate

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As a result of analysis [63] the formation area of the MC memory can be represented in the following way (figure 1.16). Above the «floating» gate, there is a control gate, which is an integral part of the process of recording/erasing data in memory. This area is directly connected to the word line (look at figure 1.14). Transversely to this line there is a line of bit rows, which is connected to drain (electron flow appears when data records from this area of transistor). The drain

is separated from source with a special substrate, which does not conduct electric current.

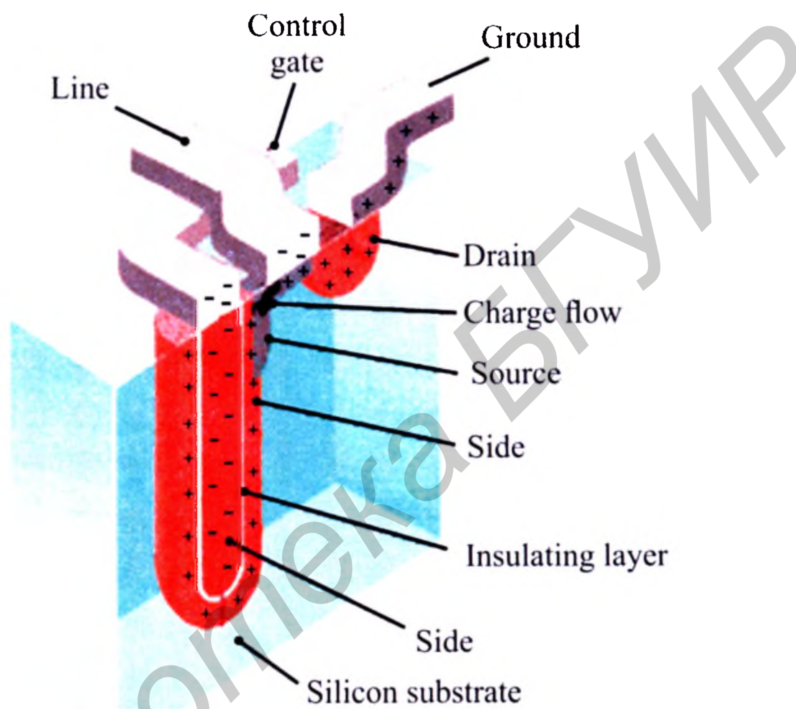

Figure 1.16. Schematic representation of solid-state semiconductor structure

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Differences between the organization of structure of the memory cells «NotAND» and «NotOR» are reflected in their characteristics. In particular, when working with relatively large arrays of data, which is an actual problem at the present stage of microelectronics, recording/erasing processes in memory of «NotAND» are carried out much faster than in memory of «NotOR». Close attention should be paid to the consistent structure of organization of cells that allows to obtain a high degree of scalability of semiconductor chip, which makes structure of «NotAND» the most significant in building of memory volumes. Also taking into

account the factor that tunneling is carried out through the entire area of the cell channel, the intensity of trapping charge per unit of area in «NotAND» is lower then in cells of «NotOR», whereby it has higher number of write/erase cycles.

1.3.4. Forms of access to the program data recorded into the built-inflash memory

The feature of flash-memory construction of modern microcontrollers can be characterized by the method of access to its cells. Basically there are three access methods: normal, packet and page [64]. All of them are used depending on the situation, because they differ in access speed and they have their own advantages and disadvantages.

In normal method, simple asynchronous reading of some specific cells is carried out. It is used in situations when it is necessary to read a small amount of information from the memory chip.

In packet access, data is read in block way, i.e. parallel. In this access method, it is possible to read the unit with size from 16 to 32 bits per one address. After reading the information, synchronization of blocks takes place in buffer, and then data is transmitted consistently. The advantage over normal access type is fast consistent reading of data. Disatvantage is slow access when reading specific memory cells.

The principle of page access reminds the principle of packet access, but data is received asynchronously. Size of the received page is 4–8 bytes. This type of access is the fastest. Its significant disadvantage is relatively slow switching between blocks.

The structure of flash memory is represented below on the example of AVR microcontroller, which is divided into two areas: section of the application program and section of the loader program. All flash memory of this type MC is divided into pages, each containing 32, 64 or 128 words.

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For example, the microcontroller with 8 KB of built-in flash memory and a page size of 32 words will have 128 pages (figure 1.17) [65].

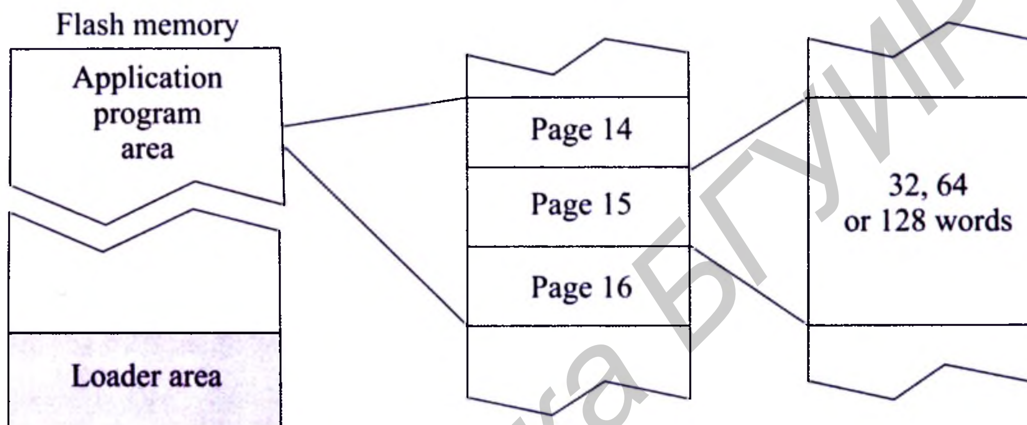

Figure 1.17. Organization of flash memory of microcontrollers

When dividing flash memory on the application memory and loading memory it can be also divided into two sections with fixed sizes: «read-while-write» (RWW) and «no read-while-write» (NRWW). These areas define what happens with the processor of MC, while one of the areas of flash memory gets a request for reading or recording. While recording or erasing in «read-while-write» area is conducted, the processor can continue working as long as the code, located in «no read-while-write» area, is executed. The size of «no read-while-write» area is always equal to the size of the largest possible loader memory. Therefore, the loader takes up the entire «no read-while-write» area or just part of it.

Division of flash memory to «read-while-write» and «no read-while-write» areas can be represented in following way (figure 1.18) [65].

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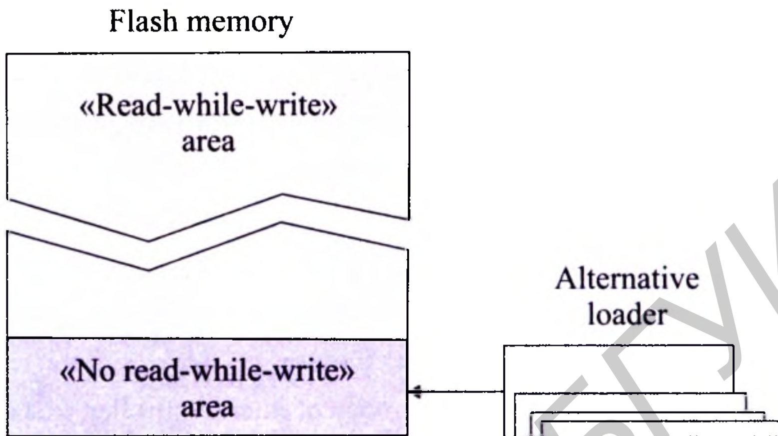

Figure 1.18. Division of flash memory to «read-while-write» and «no read-while-write» areas

However, the division of the MC's flash memory is not necessary. For example, ATmega163 and ATmega323 do not have the above-mentioned sections, because they are divided into memory of loader and memory of application program [46].

1.4. Work options of the built-in flash memory of microcontrollers

1.4.1. Process of reading data

Principle of reading data, which is recorded into the built-in flash memory of MC, is based on the process of electron tunneling. When retrieving data from memory there is no charge on a «floating» gate and control gate is supplied with a charge of positive direction. Under its impact, the free zone is created between the drain and source that allows data from memory to be read from source.

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If there is a charge on a «floating» gate, then normal voltage, which is applied when reading flash memory, is not enough. Therefore, the method of the electron injection is used, which consists in applying high voltage on control gate and source (on gate it is two times higher). Because of this applied voltage, electrons are able to overcome dielectric thin film and get to «floating» gate [66].

1.4.2. Process of erasing data

To erase information from the flash memory of microcontroller, it is enougn to apply a high positive voltage to the source (plus 6 V) and negative voltage to the gate (minus 9 V) [66]. Under its impact, negative electrons from the «floating» gate (due to the tunnel effect) go to the source. Process continues until the complete discharge of gate.

Schematically, this process is shown on figure 1.19 [66].

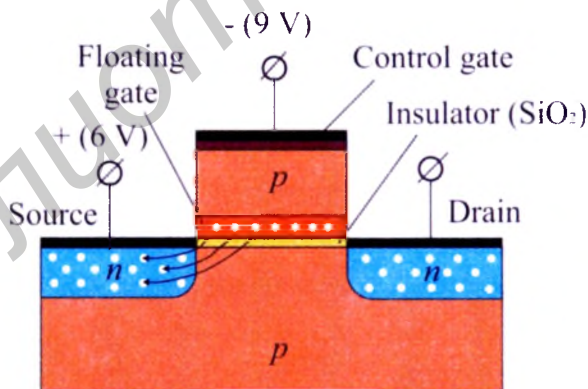

Figure 1.19. Erasure of cells from flash memory

Electron tunneling can be accelerated by applying additional negative high voltage on control gate. Due to that, electrons from the «floating» gate will be pushed toward the dielectric and time of the effect will be significantly reduced.

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1.4.3. Process of recording data

The transfer of charge to the area of «floating» gate happens due to the tunneling of electrons through the dielectric layer. This process is schematically shown on figure 1.20 1. This requires a positive voltage to be applied to the gate (plus 12 V) and to the drain (plus 7 V) [66].

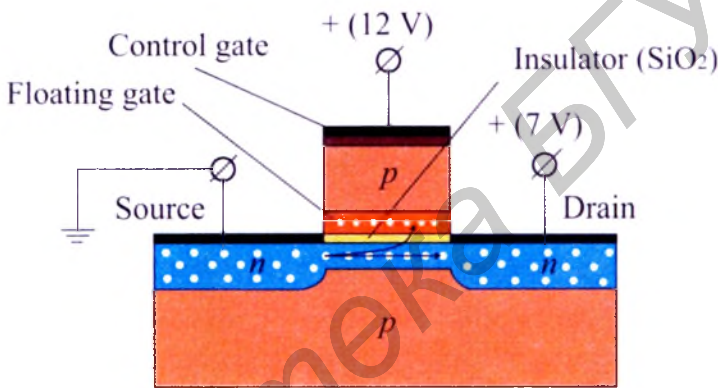

Figure 1.20. Recording of cells to the flash memory

It is worth noting, that nowadays production technology of flash memory of microcontrollers is constantly improved, new optimizing recording methods are introduced, as well as algorithms, which are aimed at the uniform use of all cells during work.

1.5. Classifications of mechanisms of injury of microcontrollers after the impact of electrostatic discharge

Nowadays the identification of inoperability causes of microcontrollers is connected with the need of searching and repairing defects, which have arised

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during manufacture process or during operating. Most of the time, which is needed to determine the defect, is spent directly on the search of defect. Due to this, quite an important task is to systematize types and mechanisms of failure inherent in modern widely used microcontrollers after the impact of static electricity discharge. This classification makes it possible to optimize and to identify with a high probability potentially unreliable current-carrying elements in the structure of integrated circuits, that in its turn will designate the need for their improvement and modernization.

Nowadays we can identify the following most common types of damage to products of semiconductor industry, due to the impact of pulsed static electricity discharge (table 1.2) [28, p. 23, table 6].

Table 1.2. Types of damages of current-carrying elements of microcontrollers caused by the impact of static electricity discharge [28, p. 23, table 6]

Elements of structure of microcontroller	Types of damage by pulses of discharge current
Traverse	Warming up of the pin by flowing current
	Spark discharge between the pin and the housing
	Electrodynamic interaction of currents of traverse and external pin
Current-carrying tracks	Melting of metallized tracks by flowing discharge current
Junctions of bipolar transistor	Full breakdown of junction
	Local breakdown
Gate of MIS structure	Breakdown of dielectric
Passive elements of MC	Burnout of metallization
	Surface breakdown of elements

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Analysis of damage mechanisms is necessary because it is important to know the causes of formation of electrostatic charge during the manufacture and operation of MC, as well as failure types under the impact of static electricity discharge to take the appropriate measures of protection. It should be noted, that availability and accumulation of electrostatic charge on any device does not cause damage or change of characteristics until electrostatic discharge occurs. Thus, prevention of occurrence of the breakdown is actual problem. If it is unable to prevent damage, two types of damage take place:

– «catastrophic» defects, which are found most easily, because a damaged device does not perform its functions. This type of damage can be divided into failures under the impact of power or current and failures under the impact of voltage, when it breaks down dielectric or destroys chip [1, p. 79; 8, p. 254];
– «hidden» («parametric») defects affect one or more parameters or cause some changes in initial characteristics that, however, may not go beyond the limits of permissible variations. It is very difficult to detect these defects because they appear only as a result of repeated discharges or during operation [1, p. 79; 8, p. 254].

Hidden defects in the structure of MC, which arise under the impact of ESD, are characterized by the emergence of small damage. However, they lead to the device failure during operation in the initial period. These defects can be detected by testing on the forced failure (for example, burn-in testing, etc.).

By the physical principle hidden defects, which are caused by the impact of ESD can be divided into three big groups [1, p. 79–85].

1. Defects of oxide. First of all, these are punctures and capture of charge by oxide. The first usually leads either to shorting or to the formation of Schottky diodes. In some cases, such defects can be undetected for a long period of time and appear only at a significant increase of temperature. The second leads to

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the shift of the threshold voltages of MOSFET-transistors and to the formation of parasitic leakage channels.

2. Defects of metallization. They appear as a deterioration of metal. Leakage currents may increase or shorting may appear as a result of such defects. In many cases the appearing conductive bridges can not affect the normal operation of circuit, and sometimes they even disappear (melt) with the overvoltage. It is believed that such defects result in a shorter lifetime of microcontrollers, in particular due to the fact that they make them more receptive and sensitive to pulsed overloads during the exploitation.

3. Defects, which are connected with melting of bulk silicon areas, that don't affect on the output parameters of MC, for example, breakdown of diffusion resistor in joint with aluminium track.

An analysis of [1, 8–11, 67] revealed the existence of six most common mechanisms of damage of MC associated with the impact of static electricity discharge (figure 1.21).

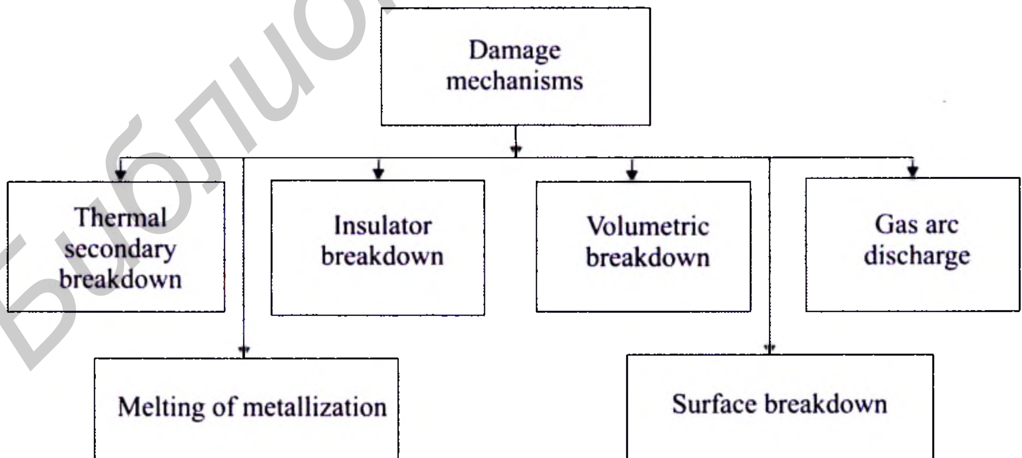

Figure 1.21. Classifications of mechanisms of damage of MC after the exposure of static electricity discharge

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The first three mechanisms of damage of MC (thermal secondary breakdown, melting of metallization and dielectric breakdown) are determined by current (power) of the discharge, the other three by voltage of the discharge.

Based on analysis of [1, 8–11, 67] we will review the most common mechanisms of damage of integrated circuits with the description of characteristics.

Heat (thermal) secondary breakdown is known as burnup (burning out) of junction [1, p.80]. With this mechanism of failure, the temperature on junction is close to the melting point of silicon (figure 1.22).

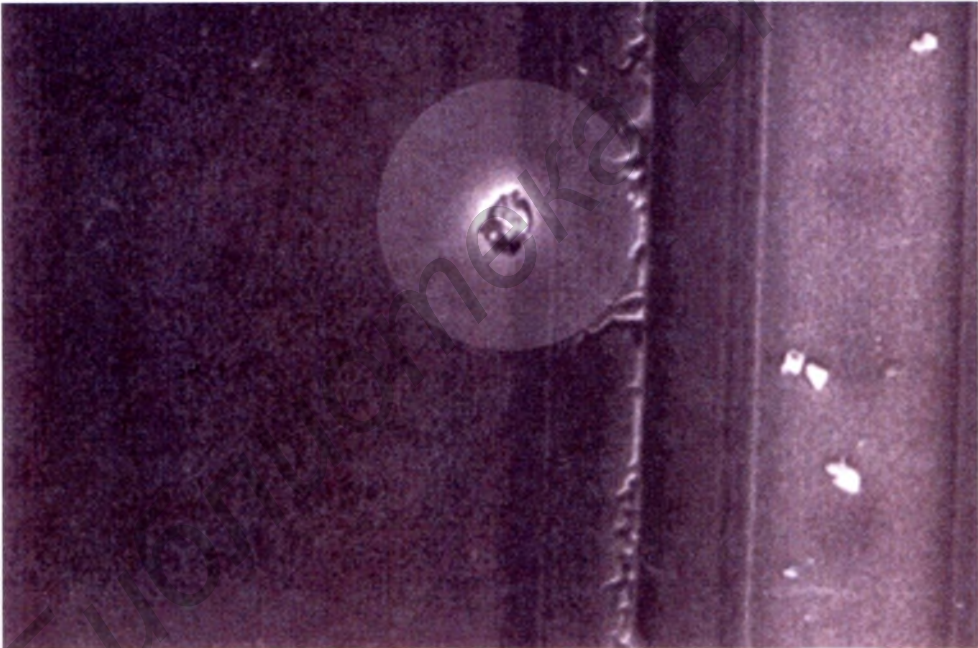

Figure 1.22. Local melting of silicon area

When temperature reaches the melting point, first melt heterogeneous «hot» spots, which leads to local melting of the silicon area. If the pulse of ESD has sufficient duration, these hot spots increase until the shorting on junction appers. Thus, this mechanism of damage of MC is associated with

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the melting of silicon in the depletion area of p-n-junction or local heating. However, thermal or heat secondary breakdown may not emerge immediately with the shorting on junction, but it can emerge later as a result of migration of electrons and ions.

Melting of metallization occurs when static electricity charge is powerful enough to melt metal of connecting tracks, as the thickness and the width of them are so small that metal melts as in the thermal fuse under the impact of the increased value of current (figure 1.23). The heating of current-carrying elements of MC occurs due to the ohmic resistance at a current density not less than 10^7 A/cm^2. Wherein the effect current density plays more sufficient role than voltage value of ESD affecting the microcontroller [1, p. 81].

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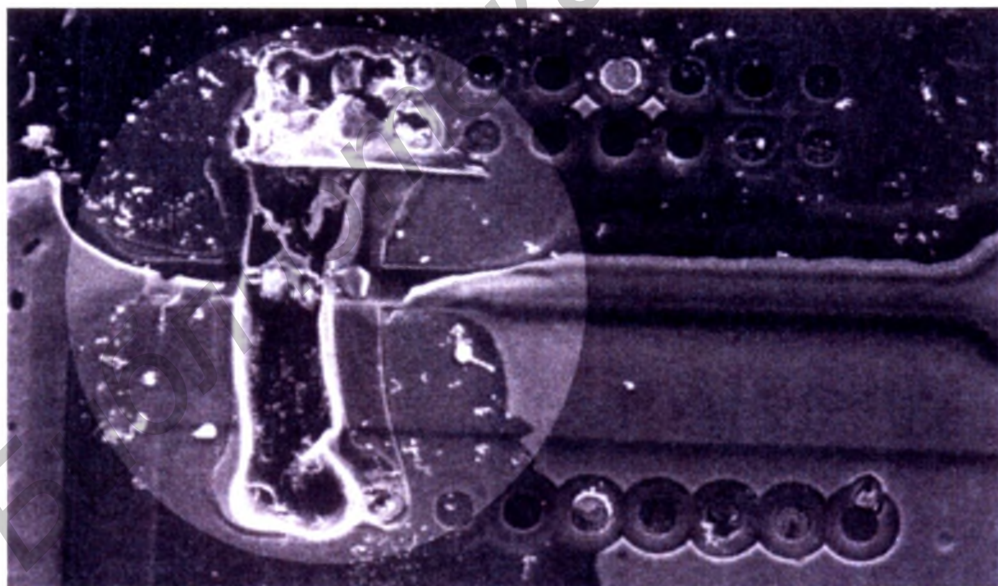

Figure 1.23. Melting of metallized tracks in structure of chip of microcontroller

Volumetric breakdown is a result of changes in parameters of junction, because of the impact of high temperatures under the exposure of discharge

current [1, p. 83–84]. This leads to rapid diffusion of impurities and to closing of junctions in volume (figure 1.24).

Insulator breakdown occurs if the value of electric field exceeds the value of field that binds electrons with the atomic nuclei [1, p. 83]. Thus, liberated electrons form an internal current, which gives the avalanche effect that destroys dielectric (figure 1.25).

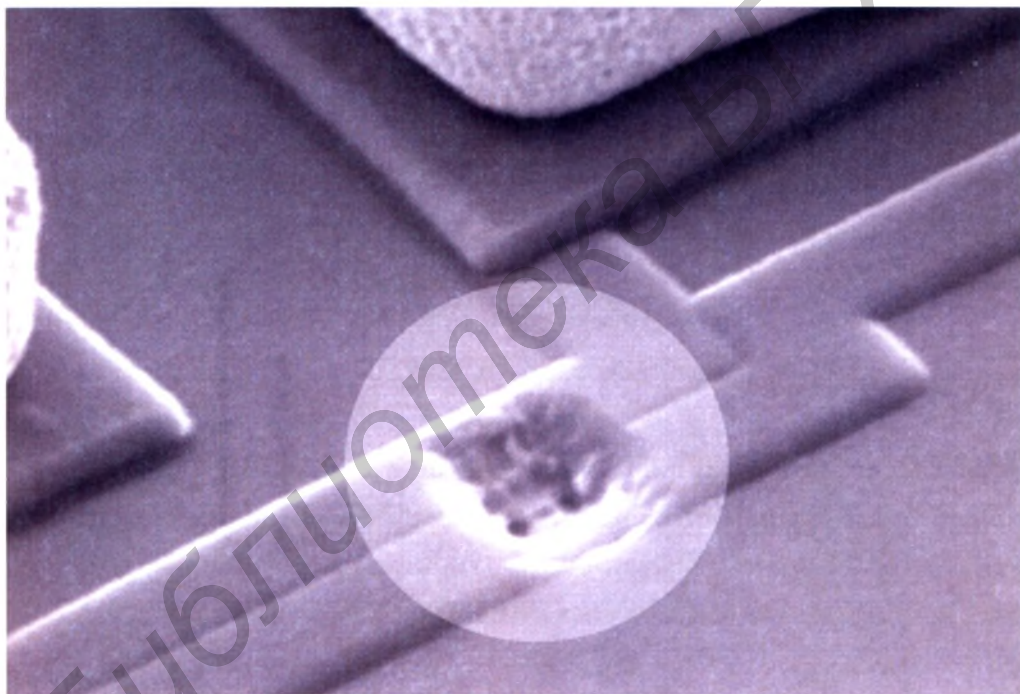

Figure 1.24. Volumetric breakdown in the structure of microcontroller

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Depending on the level of discharge energy, this phenomenon can cause shorting, reduce the allowable breakdown voltage, increase leakage currents or cause complex disorders of integrated circuit quality.

Insulator breakdown is the most common among MOSFET-transistors and capacitors of linear bipolar IC.

Figure 1.25. Breakdown of dielectric in structure of chip of microcontroller

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Surface breakdown is a failure mechanism associated with the discharge voltage and it depends on a number of parameters of the device chip, such as the levels of doping, discontinuities (ruptures) and geometry (structure, size). This phenomenon in most cases naturally leads to leakage at the junction [1, p. 83].

Gas arc discharge, which depends on voltage of failure mechanism, eventually causes the evaporation of the metal parts of chip [1, p. 83]. Arc discharge occurs in devices that contain closely placed electrodes to which an ESD voltage is applied. Voltage pulse of discharge causes the appearance of arc between electrodes, which leads to the closure.

Three most common mechanisms of failures are the following: melting of metallization on the chip, destruction of the protective layer, melting of volume silicon areas.

In most cases, the cause of failure of MC due to the impact of ESD is the combined effect of several damage mechanisms. Destruction of junction has a complex character. In this case, neither voltage, nor current alone do not play a decisive role. Their combined action influences the junction by changing its state, which in its turn is accompanied by the impact on current and voltage. This results in a point temperature increase and melting of silicon. This process becomes even more complicated due to electromigration in aluminium conductors.

As a result of analysis of a number of works devoted to the mechanisms of damage of semiconductor devices and IC, which are caused by exposure of electrostatic discharge, the following sensivity thresholds of them to this destructive impact were identified (table 1.3) [26].

Table 1.3. Sensitivity thresholds of modern SD and IC to the impact of electrostatic discharge [26]

Type of semiconductor device	Sensitivity threshold, V
MOSFET-transistor	100–200
Gallium arsenide transistor	100–200
Field-effect transistor with controlling input	140–10000
Bipolar transistor	380–7000
CMOS IC	250–3000
Linear bipolar IC	190–2500
TTL IC	1000–2500
ECL IC	500–1500
Schottky TTL IC	500–1500

Table 1.3 shows that the sensitivity threshold of integrated circuits has a wide spread. This can be explained by the dependence on the size of test elements, by manufacturing technology, choice of parameters, characterizing the suitability of IC, and by their value. For example, MOS IC with a metal gate are almost

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9 times more susceptible to ESD than the same integrated circuits with silicon gate. This happens due to the features of technological process of manufacturing silicon gate, which provides the minimum floor area of gate and reduces its capacity.

It's a common knowledge that the negative effect of ESD primarily affects the MOS- and CMOS-devices. However, the list of SD particularly sensitive to the impact of pulse of discharge is not limited only to these types. Because of ESD, degradation of input diodes is observed in digital IC. Discharges are especially dangerous for TTL IC with Schottky barrier, which breakdown at energy 2–3 times less than necessary for breakdown of TTL IC [26].

Conclusions of chapter 1

1. The analysis of types and mechanisms of the impact of electrostatic discharge on microcontrollers has shown that the discharge parameters vary over the wide range of voltages, but their development patterns are identical. When testing, the pulse discharge of current should be considered as a single electromagnetic pulse, which has individual characteristics (front, amplitude, etc.). It is designated, that during the analysis of impacting electrostatic discharge it is necessary to take into account the most important indicators such as voltage and duration of pulse, which have the major influence on the possibility of damage.

2. The analysis of design and technological features of MC has demonstrated that in case of the impact of ESD it is very hard to determine the cause of malfunction because of the presence of such functional unit as flash memory. This significantly complicates control of the functional and operational characteristics of microcontroller after exposure to pulsed discharges of current because of the need in additional analysis of damage of written code. Therefore, the development of methods of technical diagnostics of MC is a promising direction, which

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allows to identify the damage to information caused by the accidental or intentional exposure to ESD.

3. The analysis of methods of technical diagnostics of microcontrollers revealed significant shortcomings, in particular, it shows that in case of functional testing of MC rather complex system of search and detection of defects are used, also principles of diagnosis, which are not typical for the analysis of damage of flash memory, are applied. It is found that a result of exposure to a pulsed discharge of current is not only the change of static and dynamic parameters of MC, but also the probability of damage of the code, stored in memory.

4. The analysis of the studies cited by various authors has shown that methods of technical diagnostics of MC are based on the probabilistic assessment of the state of flash memory and are not adapted for taking in account characteristics of ESD. For more accurate simulation of the reaction of flash memory of modern MC to exposure of discharge it is necessary to develop new approaches to technical diagnostics of microcontrollers with recorded in the built-in flash memory data array.

5. The analysis of mechanisms of damage of MC after the impact of electrostatic discharge revealed that the greatest contribution to their appearance makes an uneven distribution of temperature gradient. It is shown that for an adequate analysis of the reaction of MC to the exposure of static electricity discharge it is necessary to take into account parameters of the incident electromagnetic pulse, basic thermophysical characteristics of current-carrying elements and their temperature dependence, as well as the topology of semiconductor chip.

It should be noted that information about technical diagnostics of MC is quite limited. It is connected with the difficulty of the analysis of all the factors that significantly affect the accuracy of used methods. All the above mentioned underlines the relevance of the research, justifies scientific significance of determining optimal modes of technical diagnostics of microcontrollers with recorded into

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the built-in flash memory program code after exposure to electrostatic discharge, that allows to give recommendation for their practical use.

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CHAPTER 2

RESEARCH OF THERMAL PROCESSES IN INTEGRATED CIRCUITS DURING THE IMPACT OF DISCHARGES OF STATIC ELECTRICITY

Development and improvement of methods of technical diagnostics, aimed at assessing operability of microcontrollers in various operating conditions, are rather laborious and require large material costs. In most cases, this is caused by the relatively high cost of experimental and diagnostic equipment.

Nowadays, the most optimal solution of minimization of the cost in obtaining data on the stability of modern microcontrollers to the exposure of static electricity is achieved by the introduction of simulation models (SM) [1, 2].

Simulation modeling is a kind of computer modeling, which is characterized by playback on a personal computer (simulation) of the functioning of a complex system under study [1, p. 5]. It allows to repeat tests of studied model many times with the necessary imput data to determine their impact on the output evaluation criteria of operating of system [2, p. 24]. Building of SM largely depends on the correct choice of physical parameters affecting the reliability of results, as well as mathematical apparatus, which allows to describe and evaluate the result with maximum adequacy [3–6].

The developed simulation model of the static electricity discharge exposure on the external pin of integrated circuit will allow to describe the process of thermal unsteadiness in the system of current-carrying elements, to track the dynamics of distribution of temperature, electric field strength and power of the electromagnetic losses, as well as to identify values of voltage of discharge

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pulse, in which damage occurs, that is very urgent task in the production of semiconductor devices.

In this chapter simulation model of a fragment of an integrated circuit is designed, the rationale for the choice of structural materials, boundary conditions, geometric shapes (rectangular and cylindrical) and dimensions of areas is given. This chapter provides the results of the distributions of temperature, electric field intensity and electromagnetic power loss in geometrically complex system, which consists of interconnected current-carrying elements with different electrical and thermal conductivity, as well as analysis of the experimental data taking into account voltage of the influencing discharge of static electricity.

2.1. Rationale for choosing the current-carrying elements of intergral circuits for the analysis of thermal unsteadiness during the impact of electrostatic discharge

Electrical circuit, through which a current pulse in the static electricity discharge flows through IC, usually includes external pins and traverses of this device, located on the chip surface current-carrying tracks, one or more series-connected junctions in random polarity and individual passive elements (thin film resistors, etc.) [7, p. 21].

Since the identification of causes of each failure in the production and, especially, during the test of IC is important in analyzing devices allegedly damaged by the impact of static electricity, it is necessary to take into account the possibility of destruction of individual elements of design by the discharge pulse. One should distinguish between types of damage that are typical for the impact of discharge on technologically faultless devices, which fully meet the requirements of technical documentation for the device, and defects, formation of which is possible only in cases when there is technological defect in their structure or

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design. The third type of defects, which should also be taken into account in the analysis, is a damage of structure or construction elements, that has a certain similarity with damage that is formed by the impact of electrostatic discharge, but due to the other causes (emergency voltage jumps in the power supply of integrated circuit on test stands, wrong setting of DC mode, etc.) [7, p. 22–23].

After the exposure of discharge current on the external pin of IC the most common is a destruction of traverse, that connects an external pin of integrated circuit with semiconductor chip, at the point of its maximum bending (figure 2.1) [8, p. 81, figure 2.10].

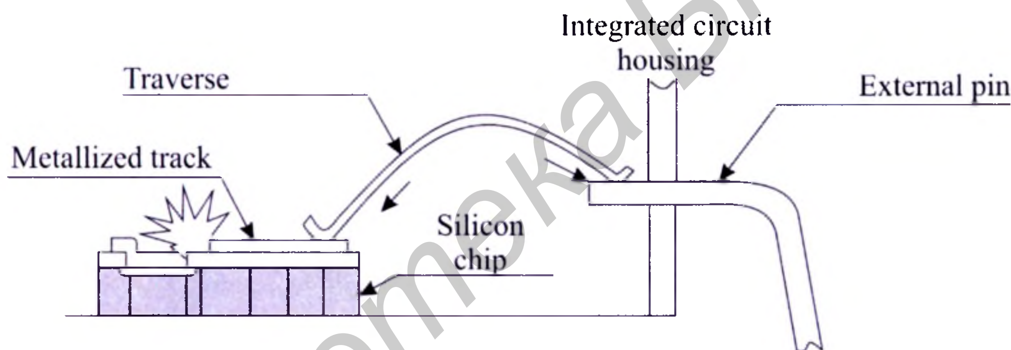

Figure 2.1. Burnout of traverse, that connects semiconductor chip with the external pins of an integrated circuit]

It also presents information that impact of pulse discharges leads to the reduction of minimum strength of welded joint and to the increase on 4–22% of amount of breaks at the place of deformation of gold traverse in the welding area on semiconductor chip and on the external pins of housing of IC.

Particular attention should be paid to the presence of technological defects of traverses, which may be unnoticed during the control (local thinnings of wire, reduced strength of termocompression bondings to the chip or to the crosspiece), because they can cause burnout of pin or its breakage at the place of thermocompression

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with the preserved junctions. Only external pins of IC can be considered as a totally resistant to static electricity discharge elements of construction.

2.1.1. The numerical model of breakdown of p-n-junction in the semiconductor chip

P-n-junction is the main element of most classes of modern integrated circuits. Its electric strength largely depends on the intensity of the internal electric field in the depletion area. During the impact of external voltage in the forward direction, potential barrier in the junction decreases, which leads to the reduction of the field intensity, and vice versa, the impact of reverse voltage on this junction causes the increase of potential barrier and increase of the field intensity in it. Therefore, the electron-hole junction is the least resistant to electrical overloads in the reverse voltage. The exceeding of critical value of voltage U_{cr} that corresponds to the limit value of the field strength Emax for this type of p-n-junction leads to its breakdown. Calculation principle of limits of field strength for various types of junctions is represented in [9].

For a sharp junction, in which the impurity concentration is discontinuously changing from the donor concentration N_d to the acceptor concentration N_a (N_d>>N_a), the electric field strength in calculated according to the formula (2.1) [7, p. 24]:

$$E_{\max} = \frac{2(\varphi_\kappa - U_{cr})}{\omega} = \left[\frac{2qN_D(\varphi_\kappa - U_{cr})}{\varepsilon\varepsilon_0}\right]^{\frac{1}{2}}, \quad (2.1)$$

where ω – the width of the space charge region.

The field strength is at maximum at the metallurgical junction and decreases linearly along the edges. The thinner the electron-hole junction, the higher the field strength in it.

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The nature of distribution of the electric field in the depletion area is particularly affected by the geometric shape of the electron-hole junction. Curvature in the peripheral part of p-n-junction results in a distortion of the electric field (figure 2.2). With decreasing of radius of curvature, the maximum field strength increases [7, p. 25, figure 12, b]:

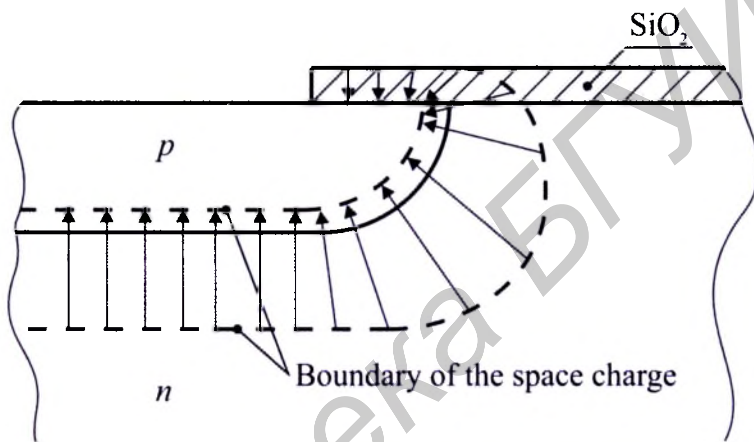

Figure 2.2. View of force lines of electric field in p-n-junction and in oxide film of integrated circuit

A noticeable effect on the electric strength of the electron-hole junction has surface condition. There are always charges on the surface of semiconductor, which arise due to the defects in the chip lattice, various contaminations and contact with protective coating. In this case the electrical properties of coatings, which insulate various elements of the structure of device and protect them from pollution, have a great importance.

The surface charge interacts with the charges of surface region of the structure. Therefore, at the exit point of p-n-junction on the surface there is a change of its width and the distortion of electric field. The biggest strength of the electric field corresponds to the point of maximum curvature. Breakdown usually initially occurs in this area.

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The principle of physical processes in the p-n-junction from moment of applying a reverse voltage drop with a finite front steepness on it, is the following. The initial increase of voltage causes the increase of concentration of microplasma – unstable, randomly appearing and disappearing outbreaks of electric breakdown at specific points of junction [10, 11]. Their uneven distribution with the subsequent growth of voltage results in the formation of mesoplasm in the center of their clot and in the simultaneous fading of all microplasmas [12, 13]. If the maximum current value is not limited by the parameters of external circuit in the safe for the device limits, then mesoplasm temperature increases to values above the melting point of the semiconductor material, and reversible electrical breakdown develops into an irreversible thermal breakdown.

According to the information from [14], channel diameter (d), that occurs during the breakdown of junction in a steady state or during the exposure of pulse with so long duration that the flow of thermal transient process can be neglected, can be expressed by the formula (2.2):

$$d = \frac{I}{2\int_{T_M}^{T} \frac{\lambda(r)}{\Phi(r)} dT(r)}, \tag{2.2}$$

where I – total current in case of breakdown;

T, T_M – temperature at the periphery of the chip and in the hottest point of junction;

λ – thermal conductivity of semiconductor;

Φ – function of potential change with distance from the center of the breakdown channel narrowing to the periphery of the chip;

r – radius vector in the polar coordinate system with the center in the middle of the breakdown channel.

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The duration of described processes is defined by the rate of increase of the applied voltage and by the thermal inertia of the semiconductor structure containing electron-hole junction. Thus, the net effect of static electricity discharge in p-n-junction (formation of microplasmas and further mesoplasm; the emergence of the local breakdown channel with specific section or the complete breakdown of junction) essentially depends on the parameters of discharge current pulse (amplitude, duration, edge steepness), value of thermal resistance and thermal transfer junction-housing characteristic.

2.1.2. Thermal processes in the traverses during the flow of discharge current pulses

Traverse of modern IC is a segment of gold or aluminium wire with thickness from 18 to 30 μm [15–23]. Due to the relatively large heat capacity of the semiconductor chip and the thermal conductivity of the external pin (crosspiece), the temperature of traverse ends during the flow of discharge current pulse is practically indistinguishable from the ambient temperature T_0, and since the length of pin exceeds its diameter at least several tens of times, the maximum temperature T_M is set in the middle of length of pin. Thus, a uniform straight rod of circular cross section, that contacts with its faces with two ideal heat sinks (the external pin and the contact pad of integrated circuit), can serve as a thermal model of the traverse, heated by pulse current of ESD (figure 2.3) [7, p. 36, figure 25].

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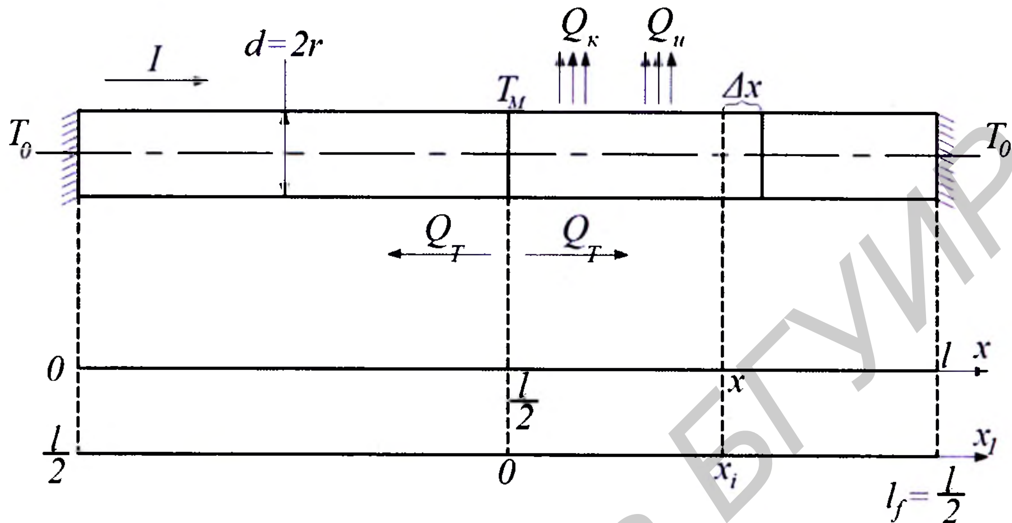

Figure 2.3. Thermal model of the traverse of integrated circuit, heated by flowing current

Heat transfer from the heated by the flowing current IC's pin can be carried out in three ways: convection, heat radiation and heat conduction along the pin. Appropriate heat flows shown on figure 2.3, are marked with Q_c, Q_r и Q_C. The amount of heat transferred per unit of time from the traverse is:

– by convection (in accordance with Newton's formula) [7, p. 36]

$$Q_c = 2\pi\alpha_c rl(T - T_0), \tag{2.3}$$

– by thermal radiation (at Stefan-Boltzmann law) [7, p. 36]

$$Q_r = 9{,}8\pi\varepsilon\left(\frac{T}{100}\right)^4 rl, \tag{2.4}$$

– by heat conduction [7, p. 36]

$$Q_C = \frac{8\lambda\pi r^2}{l}\left(T_M - T_0\right). \tag{2.5}$$

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Formulas (2.3) – (2.4) use the following denotions: λ – coefficient of thermal conductivity of material (W/m×K), l – length of the traverse (m); r – radius of wire (m); α – coefficient of heat transfer by contact kcal/(m^2×h×K); ε – emissitivity factor of the radiating body; T temperature (K).

Heat balance equation for the steady mode $P(x)Q(x) = 0$, taking into account the temperature dependence of resistivity of the material of integrated circuit's traverse, leads to the differential equation of the temperature distribution along the traverse of integrated circuit (2.6) [7, p. 36–37]:

$$\frac{\partial^2 T(x)}{\partial x^2} + \frac{I^2 \alpha \rho_0}{s^2 \lambda} T(x) + \frac{I^2 \rho_0}{s^2 \lambda} = 0, \tag{2.6}$$

where I – value of current flowing through the traverse;

s – section of traverse;

α – temperature coefficient of resistivity.

Solution of the equation of temperature distribution (2.6) takes the form (2.7) [7, p.37, equation 4]:

$$T(x) - T_0 = \frac{1}{\alpha}\left[\cos kx + \frac{1 - \cos kl}{\sin kl} \sin kx - 1\right], \tag{2.7}$$

where $k^2 = \dfrac{I^2 \alpha \rho_0}{s^2 \lambda}$.

As follows from (2.7), the maximum temperature is achieved in the section of the integrated circuit's traverse. When considering boundary conditions $T_M = T_m$, its melting current can be represented by the following equation (2.8) [7, p. 37, equation 5]:

$$I_m = 2\frac{s}{l}\sqrt{\frac{\lambda}{\alpha \rho_0}} \arccos \frac{1}{1 + \alpha (T_m - T_0)}. \tag{2.8}$$

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To consider the non-steady mode it is most convenient to represent the heat conductivity equation in the operator form (2.9) [7, p. 37, equation 6]:

$$\frac{\partial^2 T(p,x)}{\partial x^2} - T(p,x)\left[\frac{p}{\alpha^2} - \frac{I^2 \alpha \rho_0}{s^2 \lambda}\right] + \frac{I^2 \rho_0}{s^2 \lambda} = 0, \tag{2.9}$$

where T(p, x) – Laplace-Carson transform of a thermal transient characteristic of pin (see figure 2.3);

$\alpha^2 = \lambda / c\gamma$ – coefficient of thermal diffusivity of pin;

c – specific heat capacity;

γ – density of the material of pin.

Solution of (2.9) for the maximum temperature in the cross section of integrated circuit's traverse takes the following form (2.10) [7, p. 37, equation 7]:

$$T_M(p) = \frac{I^2 \rho_0}{s^2 \lambda k^2}\left[1 - \frac{1}{ch\frac{kl}{2}}\right], \tag{2.10}$$

where $k^2 = \frac{p}{a^2} - \frac{I^2 \alpha \rho_0}{s^2 \lambda}$.

Inverse transform of $T_M(p)$ cannot be expressed in terms of elementary functions and can be represented only in the form of an infinite series. However, in case of ESD and for actual values of parameters of pins, the view of thermal transient characteristic can be greatly simplified and reduced to the expression (2.11) [7, p. 38]:

$$T_M(t) \approx \frac{I^2 \rho_0}{s^2 c \gamma} t. \tag{2.11}$$

Thus, the thermal destruction of IC's traverses indicates the occurrence of overload current through them for a time much longer than the duration of the discharge pulse.

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2.1.3. The effect of electrodynamic interaction of currents of external pins and traverses during the static electricity discharge

The model, explaining the appearance of force of electrodynamic interaction of currents of traverses and external pins of IC's, is shown on figure 2.4 [7, p. 41, figure 28].

The appearance of this force is related to the fact that the thermocompression bonding of integrated circuit's internal pin to the external pin is carried out at some distance from the edge of the external pin's face, and that the wire itself may be insufficiently pressed to the internal pin [15, 21]. Since the static electricity discharge pulse is quite short, the discharge current has a high density of high-frequency components of the spectrum. Due to the action of skin effect, the penetration depth of the current into metal is about 15 μm, i.e. there is a current spreading over the face of internal pin. As a result, the area of face surface to the point of electrical contact with the wire of internal pin and the internal pin itself form a half-coil, inside which a strong magnetic field appears. The interaction of this field with the current of internal pin leads to the appearance of electrodynamic force tending to straighten a half-coil: force vector dF acts on the length of pin element dl, and points up (magnetic induction vector B inside the half-coil is directed perpendicular to the plane of figure 2.4).

The value of induction inside the half-coil in accordance to the method of images and Biot-Savart law, which are written as (2.12) [7, p. 41, equation 9]:

$$B(l) = \frac{\mu_0 I}{4\pi r_0}\left[\frac{l}{\sqrt{l^2 + r_0^2}} + \frac{L-l}{\sqrt{(L-l)^2 + r_0^2}}\right], \tag{2.12}$$

and a repulsive force according to the Ampere's law is defined as (2.13) [7, p. 41, equation 10]:

$$dF = IBdl. \tag{2.13}$$

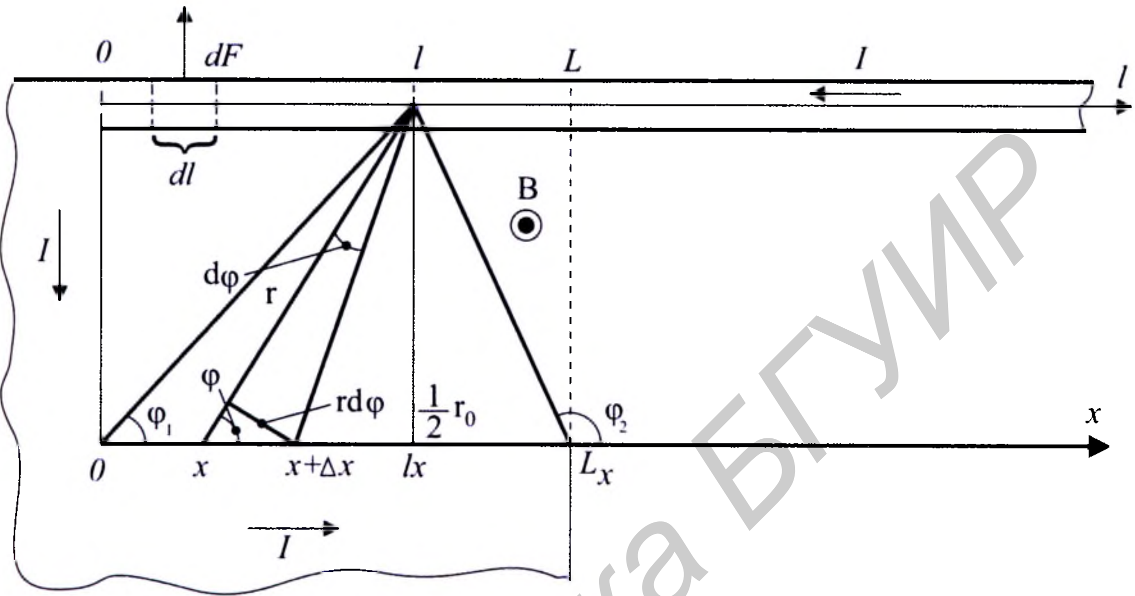

Figure 2.4. Model that illustrates the appearance of force of electrodynamic interaction of currents of traverses and external pins

Comparing (2.12) and (2.13) we get the expression (2.14), describing the distribution of load within the length of the traverse [7, p .41]:

$$q(l) = \frac{dF}{dl} = IB(l). \tag{2.14}$$

The most effective methods of reducing of the electrodynamic action of discharge current are technological methods of attaching the traverse as close as possible to the face edge of traverse and without clearance. The strengthening of contact points with polymerizable compound (epoxy compound, etc.) leads to the almost total exclusion of separation. A significant effect provides the introduction of technological control of strength of thermocompression bondings, which should have at least such a strength as traverse has.

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2.1.4. Thermal processes in the metallized tracks during the flow of current discharge pulse

Among various types of damage of IC by static electricity discharges a prominent place belongs to the effect of melting of metallized tracks, which are narrow (with the width of a few microns), thin (thickness is about 0,5 μkm), long (length is 100 μkm) strips of metallization sprayed onto the surface of the oxide protective films [16–20].

When calculating the thermal regime it is enough to consider the process of abstracting the heat flow only from the track (generally, from the most heated area of it), neglecting thermal processes of the contact pad.

Heat abstraction from the track is performed in four ways: by convection, heat radiation, heat transfer along the track and heat transfer in the depth of the semiconductor chip. The amount of heat abstracted from the metallized track per unit of time is:

– by convection (in accordance with Newton's formula) (2.15) [7, p. 46, equation 12]

$$Q_c = \alpha_c S_c (T - T_0), \tag{2.15}$$

– by thermal radiation (at Stefan-Boltzmann law) (2.16) [7, p. 46, equation 13]

$$Q_r = 4{,}9\varepsilon \left(\frac{T}{100} \right)^4 S_r, \tag{2.16}$$

– by thermal conductivity of metallized track (in accordance with the law of Fourier) (2.17) [7, p. 46, equation 14]

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$$Q_{C1} = \frac{8\lambda S}{l}\left(T_M - T_0\right). \tag{2.17}$$

Formulas (2.15) – (2.17) use the following denotions: α_c – coefficient of heat transfer by contact (W/(cm²×K)); S_c – area of surface participating in the heat exchange (m²); T, T_0, T_M –track surface temperature, ambient temperature and the temperature of track in the hottest cross section respectively (K); ε – emissitivity factor of the radiating body; S_r – area of radiating surface (m²); λ – coefficient of thermal conductivity of track (W/m×K); l – track's length (m); S – cross-sectional area (m²).

Thermal model of multilayer structures with multiple interacting heat sources on surface is very cumbersome for the analysis of dynamics of the flow of electrothermal processes. A rigorous solution of the problem of thermal transient characteristic of such model is associated with great mathematical difficulties and usually leads to the solution in form of an infinite series [116]. However, this model can be significantly simplified, if we take into account the difference between values of thermal resistance and thermal diffusivity of the individual layers and undesirable spreading of heat flow in the thin layers formed on the chip.

Based on the foregoing, we can make the following conclusions:

– silicon chip, that has a relatively small value of thermal resistance and a large thermal inertia, is an ideal heat abstraction for considerated process;
– sprayed tracks are characterized with negligible warm-up time and can be considered as instantly heating layers with a low thermal resistance;
– the most significant part of thermal resistance is concentrated in the layers of lead-silicate glass and silicon oxide, moreover the value of this resistance, during the flow of current discharge pulse through the tracks, depends strongly on the ratio between the discharge time constant and thermal time constant of these layers.

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The main way to increase the thermal stability of metallized tracks to the effects of static electricity discharge is to spray thicker and rather dense layers of metallization of materials with high electrical conductivity [7, p. 52].

2.2. Development of a model of heat transfer in the current-carrying elements of integrated circuits during the impact of static electricity discharge

Processes of emergence and spread of the temperature in the system of interconnected current-carrying elements of integrated circuit, which are caused by the action of such quasi-point source of energy as static electricity discharge, can be most accurately described by numerical (mathematical) model.

Mathematical model – the system of logical and quantitative relationships that are subjected to treatment and changes in order to determine how the system reacts to the changes, or to be precise, how it would react if it really existed [2, p. 23].

The best mean of building a simulation model of impact of static electricity on the external pin of integrated circuit on the method of contact discharge is COMSOL Multiphysics [24]. It's a powerful interactive environment that allows you to simulate almost all physical processes described by differential equations in partial derivatives, as well as to produce a numerical simulation of complex physical systems interacting with each other.

The advantage of COMSOL Multiphysics compared with widely used analogues such as ANSYS Emag [25] and especially ANSYS Maxwell [26] is that it allows the following:

– to extend the standard models, which use one differential equation, in multi physical models for the calculation of related physical phenomena;

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– to carry out modeling of physical processes, which is based on the solution of differential equations in partial derivatives and allows to solve these equations using finite element method;

– to set coefficients of differential equations in partial derivatives in the form of clear physical properties and conditions;

– to use a wide range of different mathematical methods for setting the system;

– to apply finite element analysis with the grid, taking into account the geometrical configuration of solids, and with an error control using various and additional numerical solutions.

One of the main features of the program COMSOL Multiphysics is the ability to connect models in different geometries and link models of different dimensions, which allows to describe the process of heat distribution not only in a particular current-carrying element of IC, but also in the entire system.

For the analysis of thermal unsteadiness a specialized unit was used – Heat Transfer Module [27], included in the package COMSOL Multiphysics. This module allows to solve problems with any combination of basic mechanisms of heat transfer: conduction, convection and radiation. It is used in the design of systems in which there is intense heat generation and heat transfer processes.

2.2.1. Justification of the choice of initial data for the model

For the analysis of processes of occurrence and distribution of temperature in the system of current-carrying elements of IC in the software package COMSOL Multiphysics, its model consisting of five main (excluding soldering nodes) current-carrying areas has been developed.

Based on the information presented in [16–23, 28–30], explaining the specifics of technology of assembly and installation of modern functionally complex

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devices of semiconductor industry, a model of an integrated circuit with the designation of main current-carrying elements, their configuration, physical-chemical properties, and geometrical dimensions has been developed (figure 2.5).

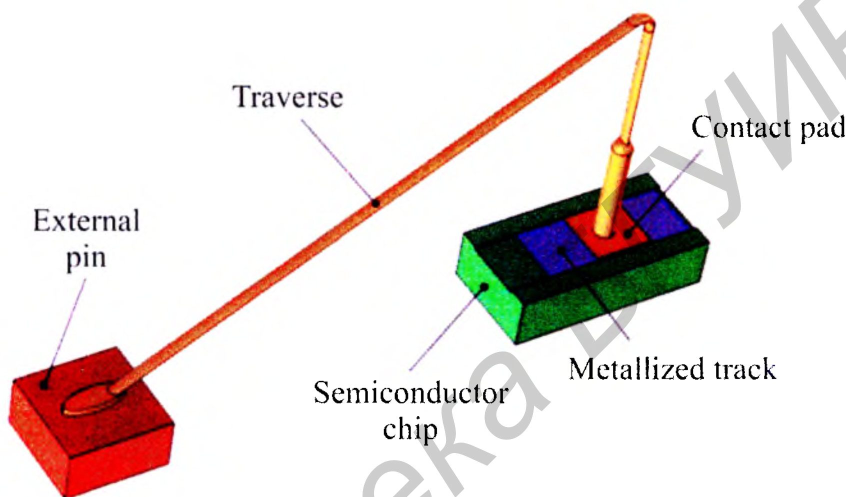

Figure 2.5. 3D model of a fragment of an integrated circuit with the designation of main current-carrying elements

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The following designations were used in the three-dimensional model: «external pin», «traverse», «contact pad», «metallized track» и «semiconductor chip».

The external pin, on which the static electricity impacts on method of contact discharge, is represented by the area made from material «Copper». Its dimensions are equivalent to the following values: length – 0,2 mm, width – 0,2 mm, height – 0,1 mm.

The traverse, which connects the external pin with the contact pad, is represented by the area «Gold». Cylindrical shape of this area has been set by the following dimensions: length – 1,5 mm, diameter – 0,025 mm.

Article [23] represents information about the most commonly used in the manufacture of IC wire brand Зл 999,9. It is produced of gold with a purity of 99,999%,

in which special additives (beryllium, copper, iron, magnesium, silver) that improve the mechanical characteristics (specific elongation – over 10%) are introduced.

The following requirements are imposed to the material of traverse: strength, ductility, corrosion resistance, good adhesion to the polymer film, etching with a gap of 50–70 μm, ease of gilding and tinning [23].

Contact pad formed on a semiconductor chip and connecting the traverse to the area «metallized track» is represented by area «Gold». Its dimensions have been set by the following values: length – 0,12 mm, width – 0,12 mm, height – 0,01 mm.

While choosing materials for the traverse and the contact pad one should take into account the risk of «purple plague» that occurs when welding aluminium with gold [23]. Purple plague is porous intermetallic compounds such as Au_xA1_y, enriched either by aluminium ($AuA1_2$), or by gold (Au_2A1) and occurring in a direct contact of aluminium and gold. The formation of this compound between the gold wire and aluminium pads causes the appearance of mechanical stresses or microcracks in this area.

Metallized track is an area on a semiconductor chip of an integrated circuit, which is represented by area «Aluminium» with the following dimensions: length – 0,3 mm, width – 0,12 mm, height – 0,001 mm.

Semiconductor chip is represented by area «Silicon». Overall dimensions: length – 0,4 mm, width – 0,14 mm, height – 0,01 mm.

The choice of materials for each of the current-carrying area is based on the most frequent use of the submitted materials in the manufacture of modern integrated circuits.

2.2.2. Construction of the calculational domain of simulation model

To simulate the process of the emergence and spread of temperature in the system of current-carrying elements of IC under the impact of static electricity

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discharge in the COMSOL Multiphysics a simplified model was constructed, the calculational domain of which is shown on figure 2.6. The number of layers is caused by the fact that the thermal processes are not considered in the soldering nodes. This would lead to the cumbersome construction of mathematical apparatus due to the specificity of thermal conductivity of alloys, as well as to long calculations.

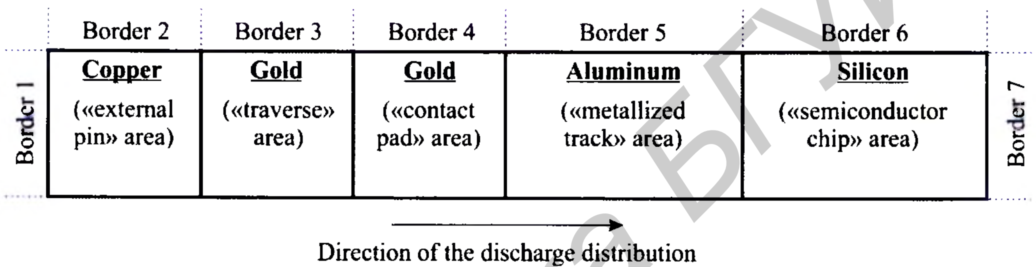

Figure 2.6. Calculational domain with defined boundaries

In each area of the calculational domain, systems of differential equations in partial derivatives are solved using numerical finite element method (FEM) [31, 32]. The essence of FEM is that the area, in which we seek a solution of differential equation, is divided into a finite number of elements. The type of approximating function is randomly selected in each of them. Beyond its element, the approximating function is equal to zero. The values of the functions on the boundaries of the elements (nodes) are the solution of the problem and are unknown in advance. Coefficients of the approximating functions are usually sought from the condition that values of neighbor functions on the boundaries of elements are equal. Then, these coefficients are expressed through the values of the functions at the nodes of elements. The system of linear algebraic equations is composed. The number of equations equals the number of unknown values at the nodes, on which the solution of the original system is sought, is directly proportional to the number of. Since each of the elements is connected with a limited number

of neighbor, the system of linear equations has a discharged form that greatly simplifies its solution.

2.2.3. Numerical description of physical processes in the system of current-carrying elements of integrated circuit

For a description of physical processes, occurring in the system of current-carrying elements of integrated circuit under the impact of static electricity contact discharge on the external pin, formulation and formalization of problems of the description of processes of heat conduction and electrical conduction was completed, taking into account the specificity of software package COMSOL Multiphysics.

Taking into account, that under the impact of ESD on the IC their failures are caused by two most common components (a sharp rise of temperature and the flow of charged particles), simulation of physical processes was based on the solution of equations of thermal and electrical conductivity.

Based on works [33–40], the change in the temperature distribution in a system of interconnected current-carrying elements of different geometrical shape can be represented by the equation of heat conductivity, which describes the heat transfer by microscopic structural material particles (molecules, atoms, electrons) during the process of their thermal motion in solids with heterogeneous temperature distribution. Its use is determined by the fact that during the impact of the discharge on the external pin of an integrated circuit there is an emergence and rapid rise of temperature, which is distributed throughout the complex system of current-carrying elements.

In this work the complex system means a system consisting of different types of elements with different types of connections [1, p. 10].

In the analysis of results of works [33–36], there was accounted the fact that the simulation model of IC was constructed of five layers (see figure 2.6), and

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the complex of solids with different thermal and physical parameters and with pronounced boundaries is called a system of solids, each part of which is a homogeneous body.

Below is a numerical description of physical processes in the system of current-carrying elements of IC through the equations of thermal and electrical conductivities.

The main law controlling the entire heat transfer is the first law of thermodynamics, which is commonly called the law of conversation of energy. However, the internal energy is rather inconvenient value to measure and use in modeling. Therefore, the basic law is usually written on base of the temperature, T. Taking into account the factor that during the flow of current the layer structure of IC partially melts, in this work the heat conductivity equation will be considered (2.18), which is described in Heat Transfer Module of software package COMSOL Multiphysics as [41, p. 31, equation 2–1]:

$$\rho C_p\left(\frac{\partial T}{\partial t}+(u\cdot\nabla)T\right)=-(\nabla\cdot q)+\tau:S-\frac{T}{\rho}\frac{\partial\rho}{\partial T}\bigg|_p\left(\frac{\partial p}{\partial t}+(u\cdot\nabla)p\right)+Q, \quad (2.18)$$

where ρ – the density, kg/m^3;

C_p – the specific heat capacity at constant pressure, J/(kg·K);

T – absolute temperature, K;

u – the velocity vector, м/с;

q – the heat flux by conduction, W/m^2;

p – pressure, Pa;

τ – the viscous stress tensor, Pa:

$$\tau=\eta\left(2S-\frac{2}{3}(\nabla\cdot u)I\right),$$

where η – viscousity, Pa·s;

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I – unit tensor;

S – the strain-rate tensor, 1/c [41, p. 31]:

$$S = \frac{1}{2}\left(\nabla \mathrm{u} + (\nabla \mathrm{u})^T\right),$$

Q – presence of heat sources other than viscous heating, W/m^3;

$\nabla \cdot q$ – divergence of vector q, i.e. $\frac{\partial q}{\partial x} + \frac{\partial q}{\partial y} + \frac{\partial q}{\partial z}$;

$(u \cdot \nabla)T$ – the scalar product of velocity vector and temperature gradient, which is defined by the expression: $\left(u_x \frac{\partial T}{\partial x} + u_y \frac{\partial T}{\partial y} + u_z \frac{\partial T}{\partial z}\right)$;

$(u \cdot \nabla) f$ – the operator of function f of the form $\left(u_x \frac{\partial}{\partial x} + u_y \frac{\partial}{\partial y} + u_z \frac{\partial}{\partial z}\right)$.

In equation (2.18) a number of thermodynamic relations have been used, which assume that mass is always constant, which means that density and velocity must be related through equation [41, p. 32]:

$$\frac{\partial \rho}{\partial t} + \nabla \cdot (\rho \cdot \mathrm{v}) = 0.$$

According to the Fourier's law, the conductive heat flux q is proportional to the temperature gradient [41, p. 31, equation 2–2]:

$$q_i = -k \frac{\partial T}{\partial x_i},$$

where k – the thermal conductivity of solids, W/(m·K).

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Taking into account that this coefficient can have different values in different directions (anisotropic), then k becomes tensor, which can be written as [41, p. 32; 42, p. 11, equation 1.2]:

$$k = \begin{bmatrix} k_{xx} & k_{xy} & k_{xz} \\ k_{yx} & k_{yy} & k_{yz} \\ k_{zx} & k_{zy} & k_{zz} \end{bmatrix},$$

and the conductive heat flux is given by [41, p. 32]:

$$q_i = -\sum_j k_{ij} \frac{\partial T}{\partial x_j}.$$

The second term on the right of equation (2.18) represents viscous (due to the internal friction) heating of fluid. This term arises from the internal viscous damping of a solid. The operation ":" is a contraction and in this case can be written in the following form [41, p. 32]:

$$\mathrm{a{:}b} = \sum_n \sum_m \mathrm{a_{nm} b_{nm}},$$

that is

$$\tau{:}\mathrm{S} \equiv \sum_{i,j} \tau_{ij} \mathrm{S_{ij}}.$$

The third term on the right of equation (2.18) represents the work of pressure and is responsible for the heationg of fluid under adiabatic compression and for some thermoacoustic effects. It is rather small and does not make adjustments.

Reordering the terms and ignoring viscous heating and pressure work puts the heat equation into a more familiar form [41, p. 33]:

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$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q - \rho C_p u \cdot \nabla T. \quad (2.19)$$

Taking into account that the velocity is set to zero, we get the basic equation of pure heat conductivity for each segment of the system of current-carrying elements of integrated circuit under the impact of static electricity by the method of contact discharge on the external pin [41, p. 33]:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q. \quad (2.20)$$

As a rule, most of the electric field work is released in the form of heat, which is described by the equation of volume power of thermal losses. According to the Joule-Lenz law the power of thermal losses in a conductor is proportional to the force of the flowing current and to the applied voltage [38].

In the system of IC, consisting of five areas, defined by specific materials, the volume power of thermal losses P is defined by the scalar product of the current density vector and the electric field intensity vector at this point [38, p. 186, equation 42.22]:

$$P = \left(\vec{j} \cdot \vec{E} \right) = \sigma \cdot E^2 = \frac{j^2}{\sigma}, \quad (2.21)$$

where j – the current density;

E – the electric field intensity;

σ – the specific electrical conductivity.

Based on the principles set out in [38], the electrical resistance of a real metal, in which there are all kinds of scattering of the conduction electrons in varying degrees, and it can be approximately represented in the form of two terms:

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$$\rho_n = \rho_0 + \rho(T), \tag{2.22}$$

where ρ_0 – part of the specific electrical resistance caused by scattering of electrons on static defects at t_0 = 0 °C;

$\rho(T)$ – part of the specific electrical resistance caused by scattering of electrons on phonons.

Taking into account that the IC test on resistance to static electricity using the method of contact discharge in accordance with the requirements of OST 11 073.013–2008 [43] is carried out in laboratory conditions, the interaction of electrons with lattice phonons (electron-phonon scattering) occurs at room temperature. Well-known linear dependence of specific electrical resistance of metals on the temperature is well conditioned by the scattering mechanism:

$$\rho = \rho_0 (1 + \alpha \Delta T), \tag{2.23}$$

where α – the temperature coefficient of specific resistance;

$\Delta T = T - T_0$ – temperature.

Taking into account given above formulas (2.21) – (2.23), the volume density of power of heat release can be represented as follows [44, p. 31]:

$$P = \rho_0 \cdot j^2 \left[1 + \alpha (T - T_0)\right].$$

Based on the analysis of physical properties of each material represented in [45–50] for each area according to figure 2.5 were set certain numerical values corresponding to the parameters for each material used in microelectronics in design and manufacture of integrated circuits (table 2.1).

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Table 2.1. The numerical values of the parameters for a particular area of the system of current-carrying elements of integrated circuit [45–50]

Area	Material	Values of physical parameters of material			
		Density, ρ, kg/m^3	The specific heat capacity C_p, J/kg · K	Specific electrical resistance, ρ_0, Ω · m	The temperature coefficient of specific resistance, α, 1/K
1	2	3	4	5	6
The external pin	Copper	8800	385	$1.72 \cdot 10^{-8}$	$3.80 \cdot 10^{-3}$
Traverse	Gold	19320	130	$2.25 \cdot 10^{-8}$	$3.90 \cdot 10^{-3}$
Contact pad	Gold	19320	130	$2.25 \cdot 10^{-8}$	$3.90 \cdot 10^{-3}$
Metallized track	Aluminium	2700	920	$2.69 \cdot 10^{-8}$	$4.30 \cdot 10^{-3}$
Semiconductor chip	Silicon	2330	800	$2.3 \cdot 10^{3}$	$1.70 \cdot 10^{-3}$

Presented numerical values of the physical parameters significantly simplify the calculation of equations of heat and electrical conductivity.

2.2.4. Justification of the choice of the boundary conditions

In describing the physical processes occurring in the current-carrying elements of IC because of the impact of ESD, a series of boundary conditions (BC) was set to solve the equations of thermal and electrical conductivity.

For the heat equation, BC's for all of the computational area borders (see figure 2.5) are set as the heat flow, in which the respective values of thermal conductivity (k) are equivalent to the values given in the table 2.2.

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Table 2.2. The boundary conditions for the heat conductivity equations [45–50]

Parameter	Area	Material	Boundary	Numerical value, *W/(m·K)*
The coefficients of thermal conductivity	The external pin	Copper	1	401
	The external pin	Copper	2	401
	Traverse	Gold	3	320
	Contact pad	Gold	4	320
	Metallized track	Aluminium	5	203,5
	Semiconductor chip	Silicon	6	126
	Semiconductor chip	Silicon	7	126

For the electrical conductivity equation boundary conditions were set for each border in the following way:

– for border 1 – as test voltage (table 2.3);
– for borders 2, 3, 4, 5 and 6 – as electrical insulation;
– for border 7 – as electrical potential equal to zero.

Table 2.3. Parameters of the pulse of discharge current [43]

The degree of hardness	Test voltage, kV	The current of first maximum ±10%, A	Rise time, t_r, ns	Discharge current (±30%) at 30 ns, A	Discharge current (±30%) at 60 ns, A
1	2	7,5	from 0,7 to 1	4	2
2	4	15	from 0,7 to 1	8	4
3	6	22,5	from 0,7 to 1	12	6
4	8	30	from 0,7 to 1	16	8

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In the process of meshing the spatial sampling mesh of the system of current-carrying elements of IC, an area «traverse» has a mesh grain 3 times less than in other areas. This is due to the fact that this area is sufficiently thin (25 μm), and at the same time has the greatest length in comparison with the other areas. Introduction and consideration of this feature allowed to perform the necessary calculations more accurately and to obtain the most accurate result.

2.3. Analysis of the results of modeling of thermal processes in the system of current-carrying elements of integrated circuits after the impact of static electricity discharge

Taking into account the features of the testing of integrated circuits on sensitivity to ESD represented in [51, 52], the ambient temperature in the laboratory is (25 ± 10) °C (288–308 K).

As a result of simulating we obtained the value of temperature distribution in the current-carrying elements of IC with the definition of its maximum value for each area. The obtained temperature values show how much the temperature rises in the current-carrying elements at their initial value equal to ambient temperature (figure 2.7).

It is found that due to the impact of electromagnetic pulses with the duration of 0,7–1 ns, the value of the temperature gradient in the multilayer (five areas) system of current-carrying elements may change in range between 3 and 33% for the adjacent layers and it strongly depends on the thermal conductivity of each element. The obtained value of the temperature for the considered element is average. This indicates that these values should be used for the preliminary determination of the average temperature of the considered element, and then the local overheating should be found in particular current-carrying element taking into account the calculated temperature.

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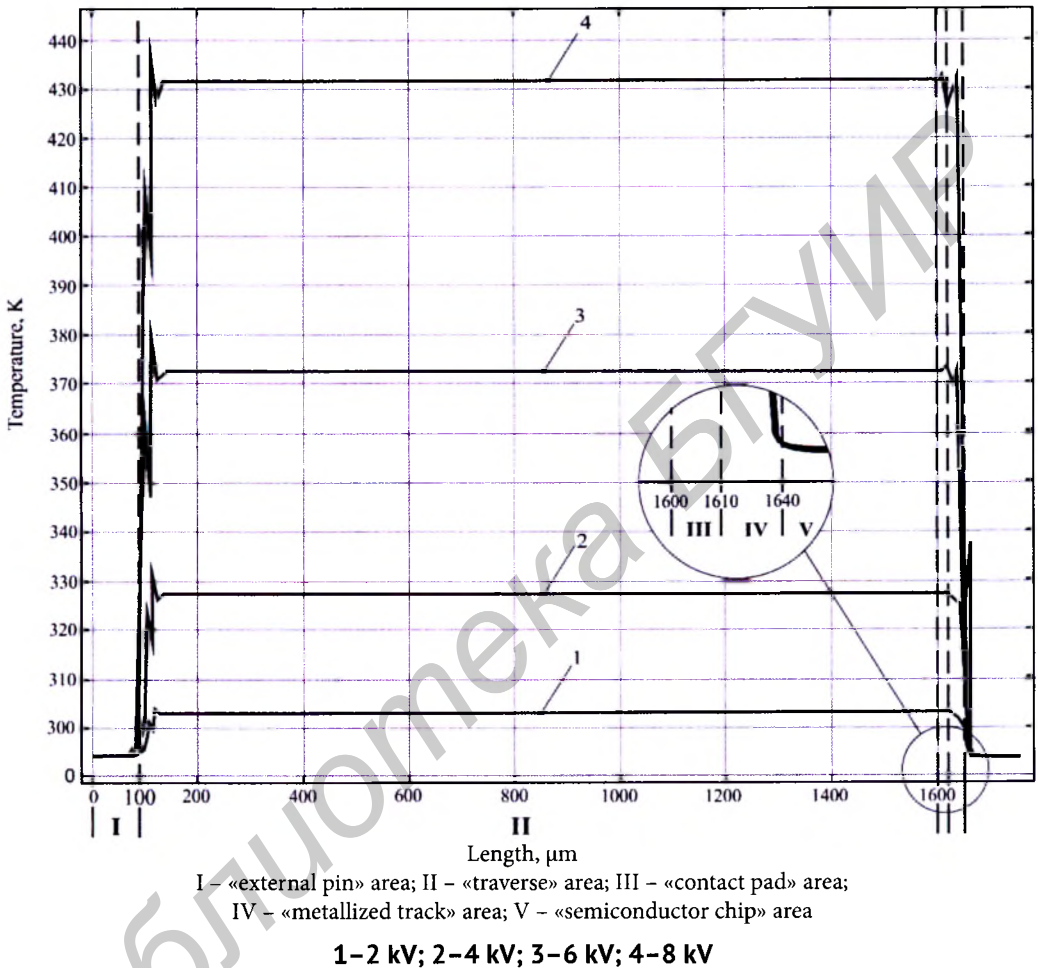

1–2 kV; 2–4 kV; 3–6 kV; 4–8 kV

Figure 2.7. The temperature distribution in the system of current-carrying elements of IC at different voltages of static electricity discharge

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Based on the experiment it was found that during the contact impact of ESD with voltage from 2 to 8 kV, the maximum temperature of current-carrying areas of IC is in the range from 300 to 430 K.

The use in the process of simulation of the temperature distribution taking into account thermal conductivity of each segment of the system of IC's

current-carrying elements as a result of the contact impact of pulsed current discharge allows to get more accurate temperature values in their volume and the form of its distribution.

The experiment revealed that the temperature change in each area is linear. The greates changes in temperature are observed between such adjacent areas as «external pin – traverse» and «traverse – metallized track». The temperature difference in these areas varies from 10 K (at a discharge voltage of 2 kV) to 140 K (at a discharge voltage of 8 kV).

It was found that the dependence of the temperature distribution on the voltage of the affecting static electricity by the contact discharge method has an identical shape. That leads to the conclusion that when changing the voltage of static electricity discharge the most likely areas of local heating stay the same («traverse» and «metallized track»).

As a result of carried out experiment to the impact of contact static electricity discharge of the external pin with voltages 2, 4, 6 and 8 kV we obtained the distribution of the electric field strength in each current-carrying element of IC with the identification of its maximum value (figure 2.8).

The analysis of received distributions revealed that the value of the electric field strength in the system of current-carrying elements of IC after the impact of ESD can change in range from 10,5 to 44 kV/m for the adjacent layers and it greatly depends on the physical properties of each element.

The simulation has experimentally revealed that the change of the electric field strength in each area is linear. The highest value of the electric field strength difference is observed between such adjacent areas as «external pin – traverse» and «traverse – metallized track». The differences of the electric field strength in these areas range from 10,5 kV/m (at the discharge voltage of 2 kV) to 44,5 kV/m (at the discharge voltage of 8 kV).

The resulting dependences of the electric field strength from the discharge voltage taking into account physicochemical properties and geometrical features

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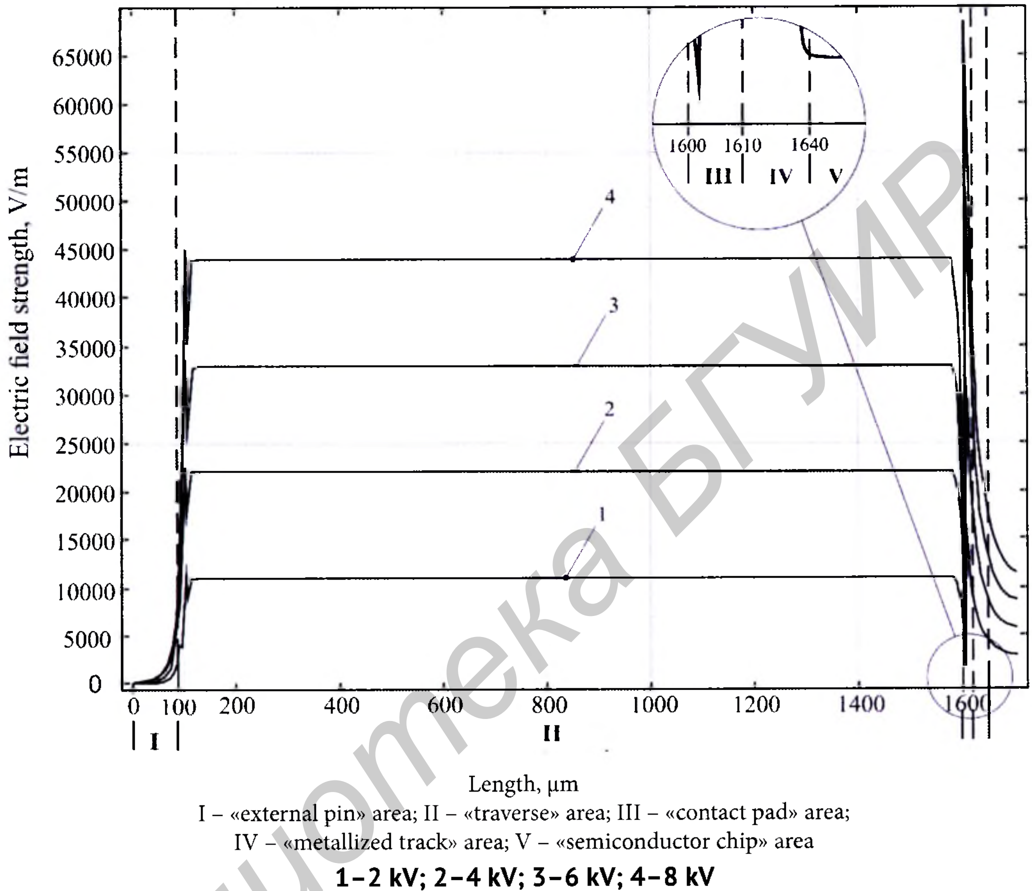

I – «external pin» area; II – «traverse» area; III – «contact pad» area; IV – «metallized track» area; V – «semiconductor chip» area

1–2 kV; 2–4 kV; 3–6 kV; 4–8 kV

Figure 2.8. The distribution of the electric field strength in the system of current-carrying elements of IC at different voltages of ESD

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During the research on contact impact of ESD on the external pin with voltages of 2, 4, 6 and 8 kV we obtained the distribution of electromagnetic losses power in each current-carrying element of integrated circuit with the identification of its maximum value (figure 2.9).

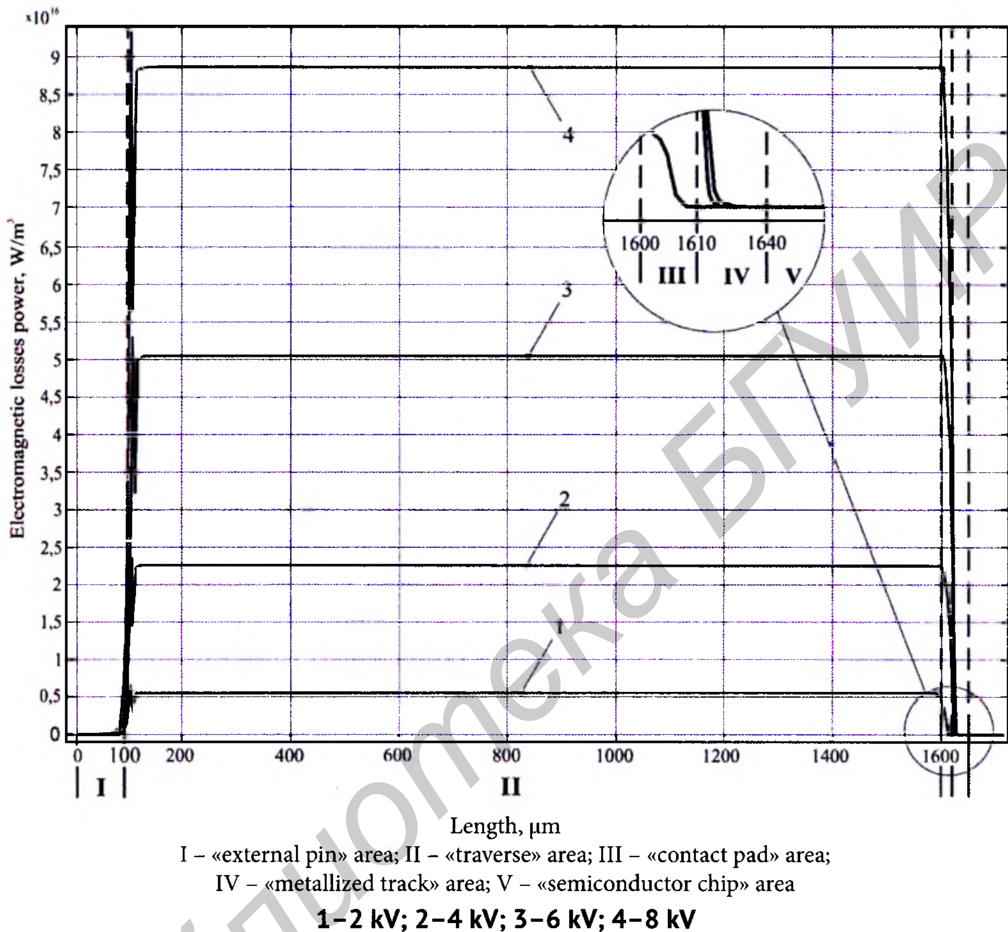

Figure 2.9. The distribution of the electromagnetic losses power in the system of current-carrying elements of integrated circuit at different voltages of static electricity discharge

The analysis of simulation results revealed that the power value of electromagnetic losses in a multilayer system of current-carrying elements as a result of impact of current pulses with duration of 0,7–1 ns can change in range from $0{,}45\times10^{16}$ W/m³ (at the discharge voltage of 2 kV) to $9{,}3\times10^{16}$ W/m³ (at the discharge voltage of 8 kV) for adjacent layers and it strongly depends on physicochemical properties of each element.

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During the experiment it was found that in the contact impact of static electricity discharge with voltage from 4 to 8 kV, the maximum power of the electromagnetic losses in the system of current-carrying areas of IC is in the range between $0,5\times10^{16}$ and $8,7\times10^{16}$ W/m^3.

It was found that the change of power of electromagnetic losses in each area is linear. Its greatest differences are observed between the materials «Cu – Au» and «Au – Au», which range from $0,4\times10^{16}$ W/m^3 (at the discharge voltage of 2 kV) to 9×10^{16} W/m^3 (at the discharge voltage of 8 kV).

Figures 2.10–2.17 show the results of photomicrography of damages of current-carrying elements of IC, confirming the adequacy of the simulation model. The analysis of these figures reveals that the area of «metallized track» is the most vulnerable to the impact of electrostatic discharge.

The results of photomicrography of damages of IC were obtained usind hardware and software system for digital photos, the main technical characteristics of which are given in the Appendix B.

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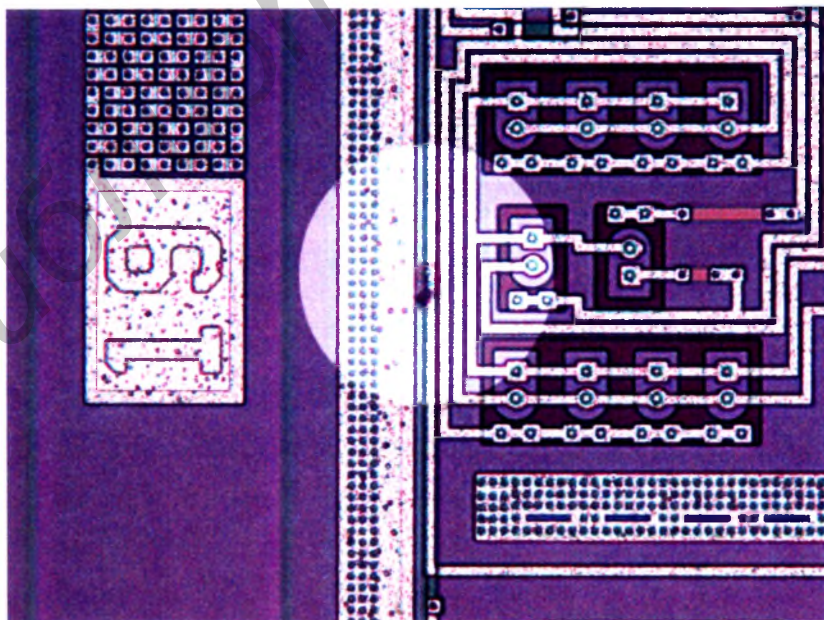

Figure 2.10. Melting of the metallization area at U_{ESD} = 2 kV (Scale 100:1)

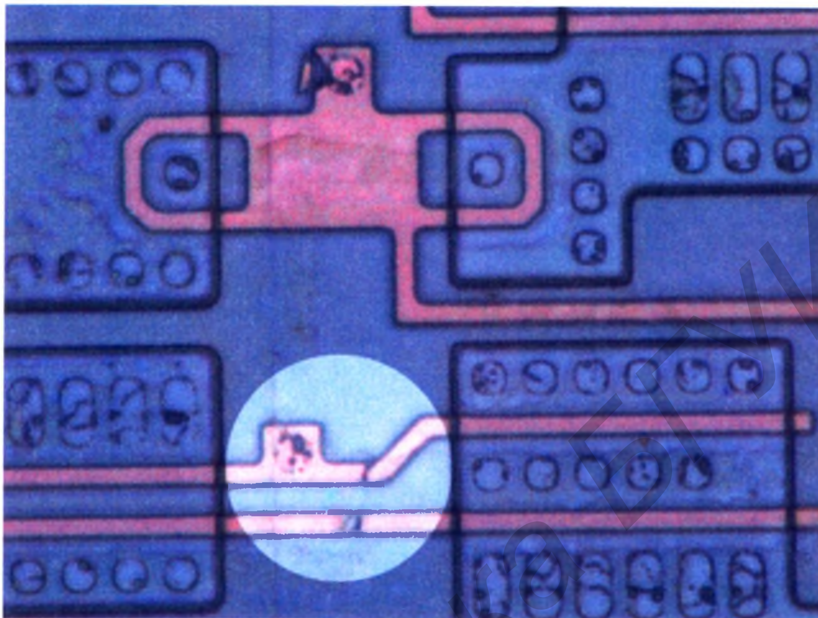

Figure 2.11. Damage of the metallized tracks at U_{ESD} = 2 kV (Scale 100:1)

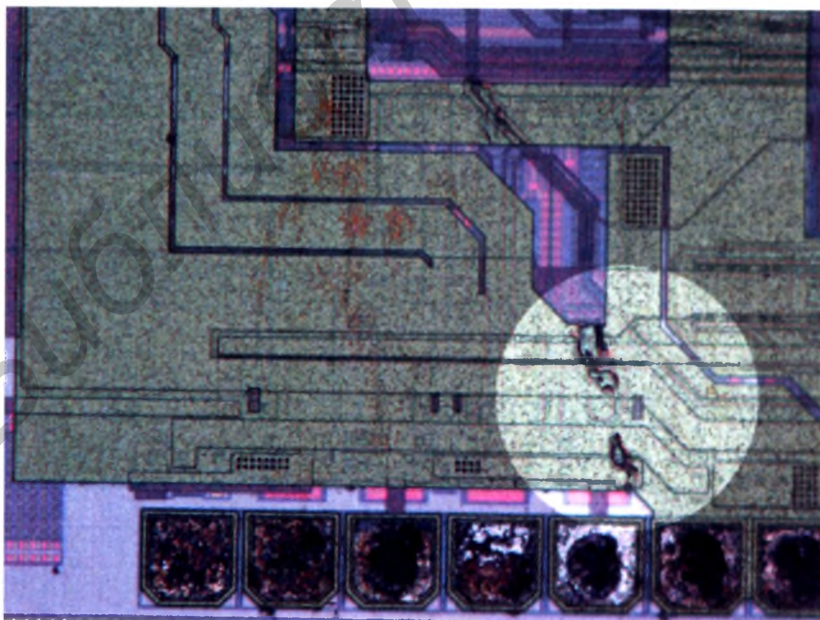

Figure 2.12. Melting of the metallization area at U_{ESD} = 4 kV (Scale 100:1)

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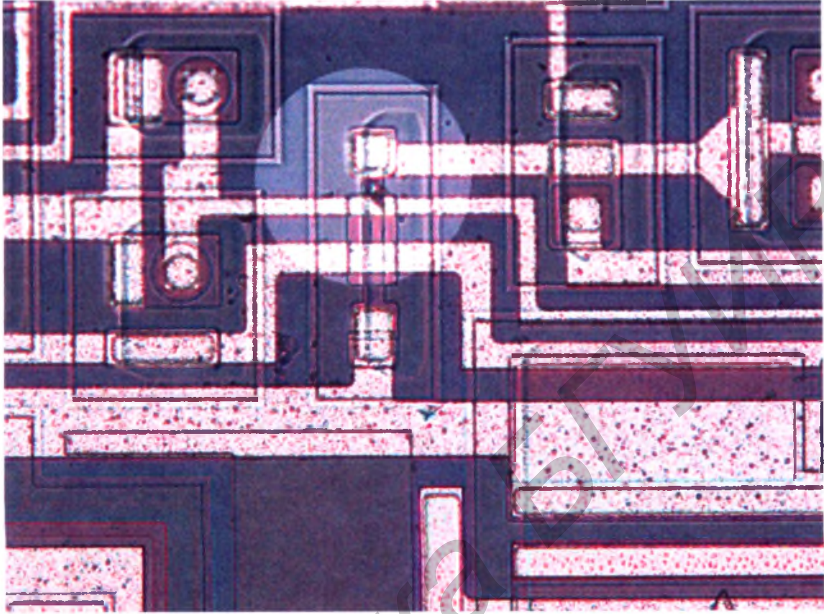

Figure 2.13. The emergence of short-circuit between two metallized tracks with damage of the structure of silicon chip at U_{ESD} = 4 kV (Scale 100:1)

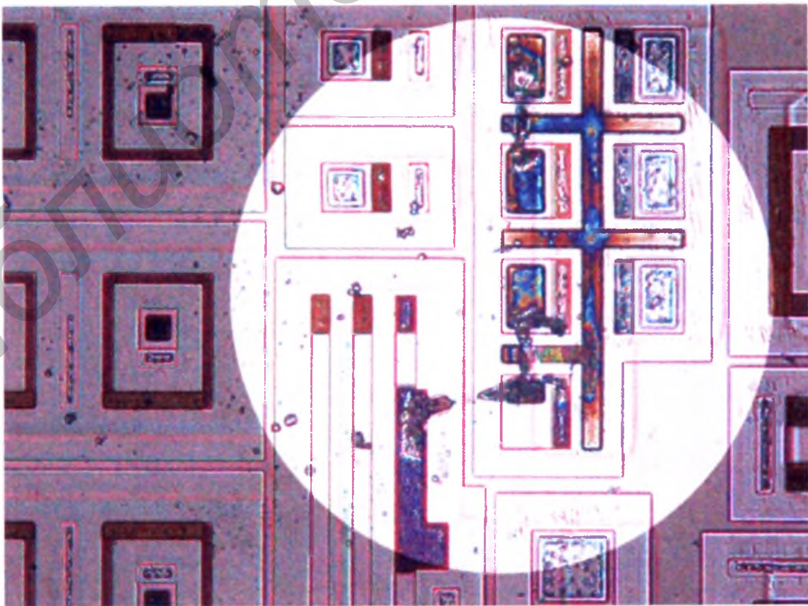

Figure 2.14. Melting of the metallization area with damage of the structure of silicon chip U_{ESD} = 6 kV (Scale 100:1)

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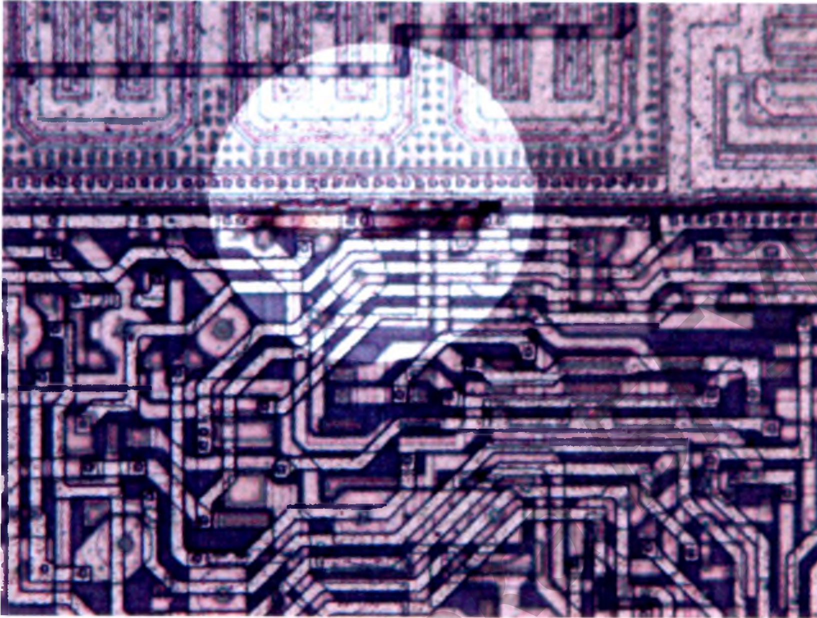

Figure 2.15. Damage of the metallization area at U_{ESD} = 6 kV (Scale 100:1)

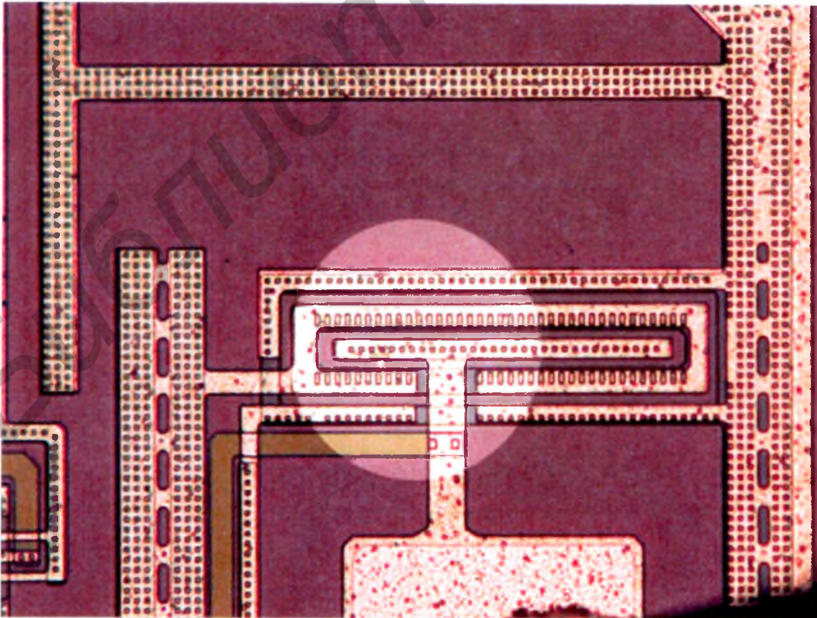

Figure 2.16. Damage of the protective element built in the structure of silicon chip of integrated circuit at U_{ESD} = 8 kV (Scale 100:1)

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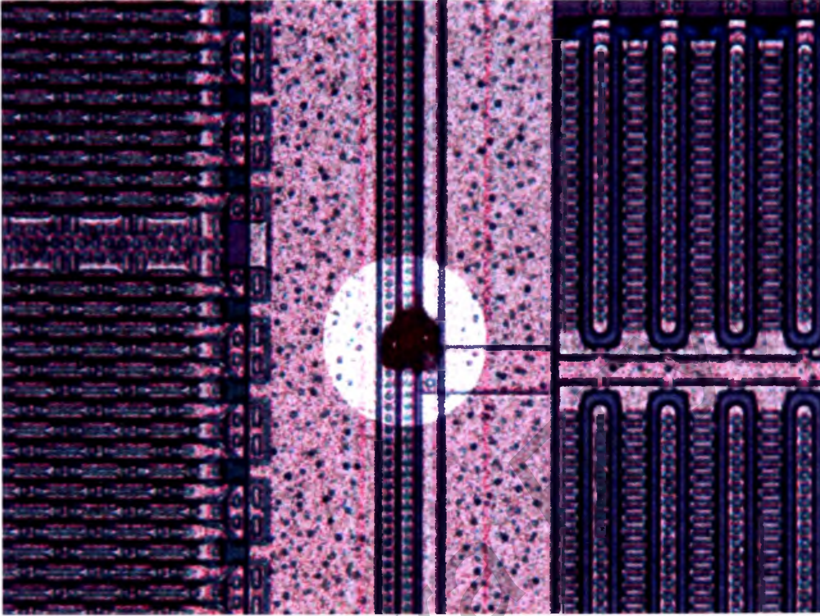

Figure 2.17. Melting of the metallization area at U_{ESD} = 8 kV (Scale 100:1)

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Based on the simulation model of IC, it was found that the values of temperature, field strength and power of electromagnetic interferences in the area of the maximum bending of traverse are higher. The numerical values of these parameters are presented in the Appendix C.

2.4. Analysis of the results of modeling of thermal processes in the system of current-carrying elements of integrated circuits after the contact impact of static electricity discharge at the maximum voltage from the operator

In accordance with the current standards of the Republic of Belarus [51–54], the maximum value of the discharge voltage from the operator is 15 kV. Also, these documents provide the indication error of the output voltage from the test

equipment of ±5%. In this regard, in the modeling of the impact of static electricity on the external pin of IC values for voltages of discharge pulse were calculated, equaling to (15±0,75) kV.

Figures (2.18) – (2.20) represent the results of modeling of the emergence and spread of thermal processes in the system of current-carrying elements of IC at the discharge voltages at 14,25 kV, 15 kV, 15,75 kV.

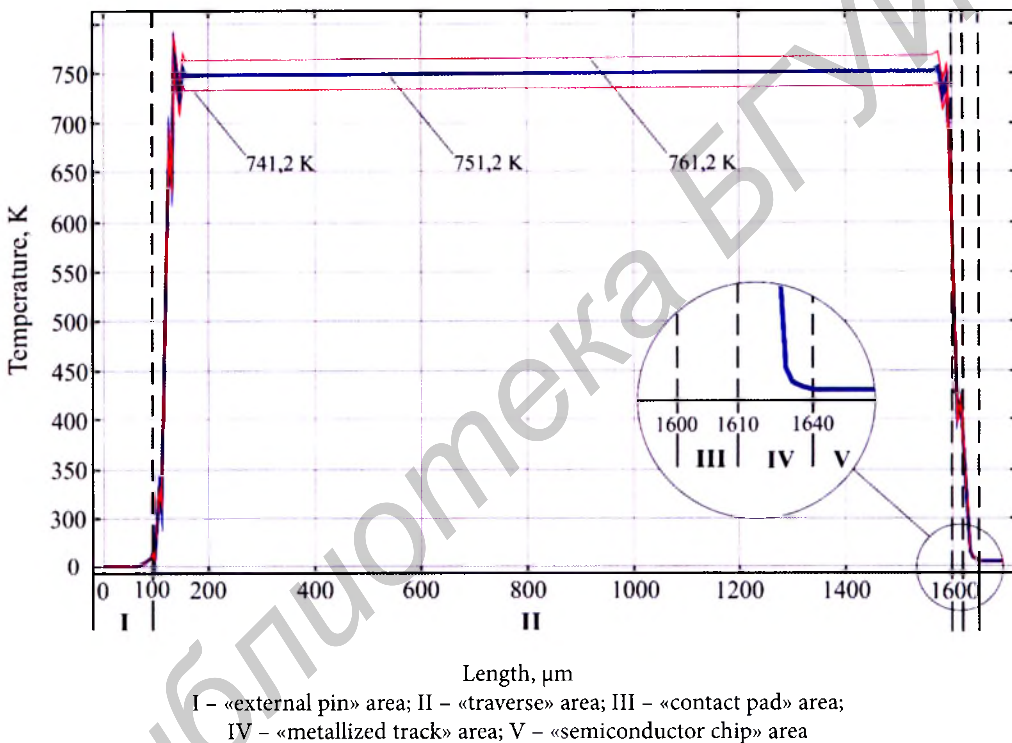

Figure 2.18. Temperature distribution in the system of current-carrying elements of IC at the maximum voltage of the static electricity discharge from the operator

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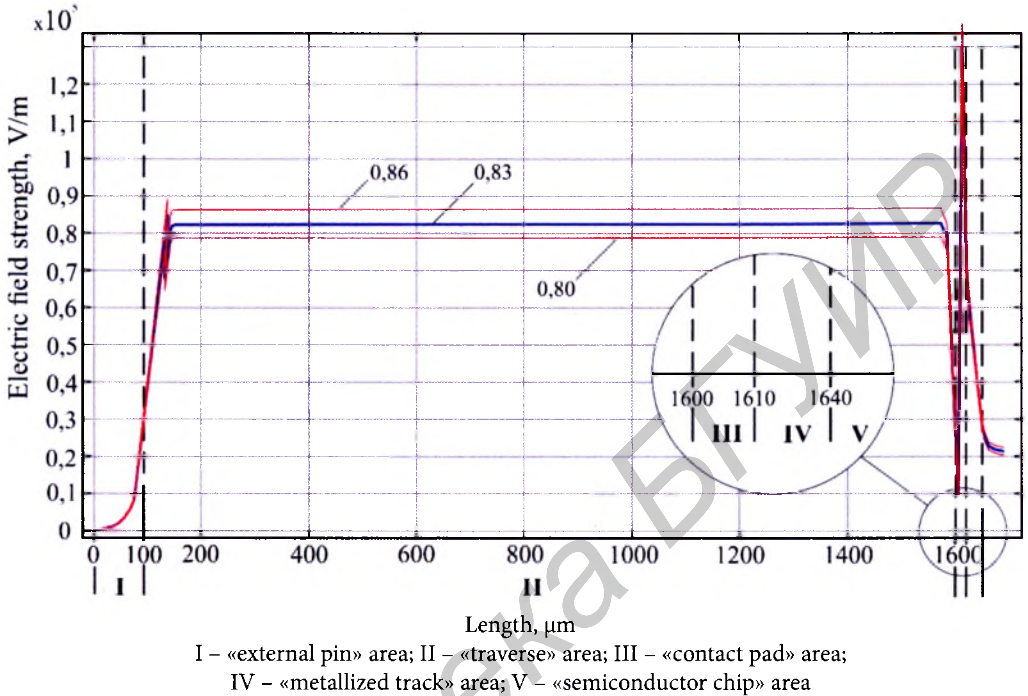

Figure 2.19. Distribution of the electric field strength in the system of current-carrying elements of IC at the maximum voltage of the static electricity discharge from the operator

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In the analysis of the results of modeling (see figures 2.18–2.20), it was found, that the maximum value of temperature (790 K at U_{ESD} = 15,75 kV), of electric field strength (0,89×10^5 V/m at U_{ESD} = 15,75 kV) and of electromagnetic losses power (3,24×10^{17} W/m^3 at U_{ESD} = 15,75 kV) are located in area of contact «external pin – traverse». It is shown that in the test the resulting values may differ on 5%.

Continuous growth of complexity of the developed IC, global trend towards submicron technology, face of fierce competition in the global market require significant effort to obtain complex information about the used materials, parameters of the microelectronic products and other objects. Due to that, information

obtained as a result of experiments, describing the process of thermal nonstationarity in the system of current-carrying elements of IC as a result of contact impact of ESD, will allow to analyse a wide range of physical parameters of designed integrated circuits, in particular it is possible to obtain information about prospective materials, about optimization of geometrical shapes of elements, etc, quickly and reliably.

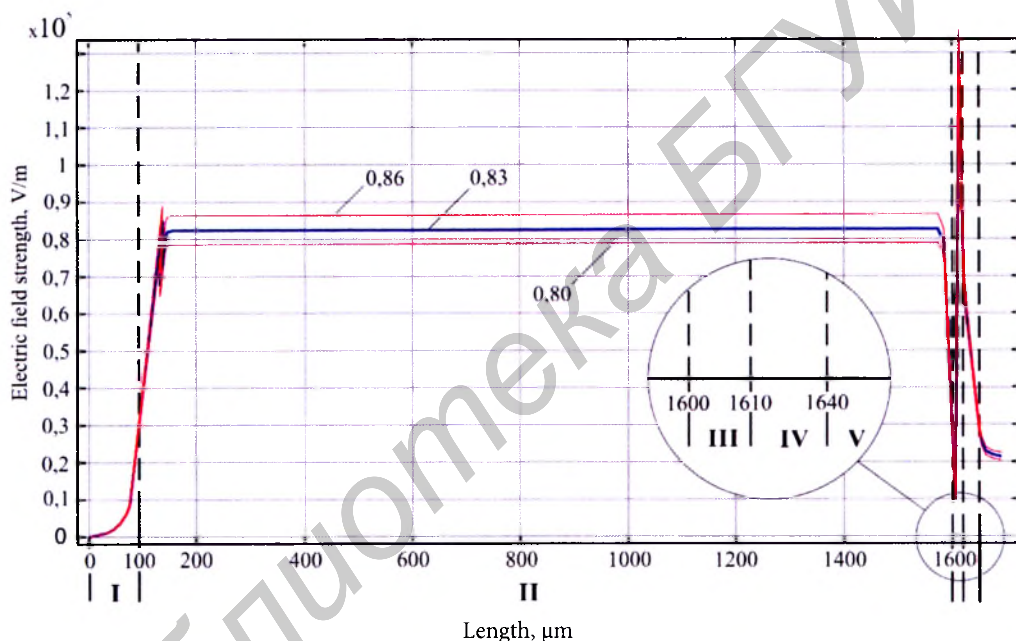

Figure 2.20. Distribution of the electromagnetic losses power in the system of current-carrying elements of an integrated circuit at the maximum voltage of the static electricity discharge from the operator

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Conclusions of chapter 2

1. It is shown, that the analysis of thermal nonstationarity in the complex system of current-carrying elements of integrated circuit, which is formed as a result of the impact of contact discharge of static electricity, is optimally performed by solving the equations of thermal and electrical conductivities. This allows to avoid the lengthy computations without significant effect on the accuracy of the results.

2. It is shown, that in each current-carrying area of integrated circuit the distribution of temperature, of electric field strength and of electromagnetic power losses at specific values of voltage of the affecting discharge of static electricity is carried out identically and is described by linear relationship, at the same time the main difference is the relationship of the discharge voltage to the thermal conductivity of the specific current-carrying element.

3. It was experimentally established that the contact impact of static electricity discharge (at voltage of 2 to 8 kV) on the external pin results in the change of temperature from 300 to 430 K, the change of the electric field strength in range of 11 300–44 200 W/m and the difference in the electromagnetic losses power is 4,4×1016 W/m^3. Also the temperature difference was determined on the contact «external pin – traverse» and «traverse – contact pad», which is in the range from 10 K (at a discharge voltage of 2 kV) to 140 K (at a discharge voltage of 8 kV).

4. The experiments revealed that during the contact impact of pulsed current discharge at voltage of 15 kV in the area of maximum bending of traverse of integrated circuit the value of temperature, of electric field strength and of electromagnetic losses power is greater in 2,53, 2,49 and 6,2 times respectively, than in straight area.

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CHAPTER 3

RESEARCH OF THE IMPACT OF ELECTROSTATIC DISCHARGE ON THE CHARACTERISTICS OF MICROCONTROLLERS WITH BUILT-IN FLASH MEMORY

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In the development of control methods of functionality and performance of microcontrollers it is advisable to consider the following system of inputs and outputs of informative parameters [1, 2].

One part of the system inputs is p-dimensional vector of parameters of MC $\vec{X}$, which can be divided into a plurality of defining parameters (parameters that significantly affect the change of output parameters of integrated circuit) and not defining parameters (parameters that do not significantly affect the change of output parameters of integrated circuit).

Another part of inputs is represented by μ-dimensional vector of input actions $\vec{Z}$. This vector is a complex of control actions on MC, each of which is characterized by its parameters.

At the same time χ-dimensional vector of destabilizing actions $\vec{f}$, which is determined by the actual operating conditions of the test microcontroller.

On the output of MC m-dimensional vector of output parameters $\vec{y}$ is observed, which depends directly on the parameters incoming from the inputs of the system of technical diagnostics.

Thus, the testing scheme of modern microcontrollers can be represented in the following way (figure 3.1) [2, p. 15, figure 1.1].

Thus, connection of inputs and outputs of the diagnosed microcontroller can be described by the following equation (3.1) [2, p. 15];

$$y = W(x, z, f), \tag{3.1}$$

where W – connection operator.

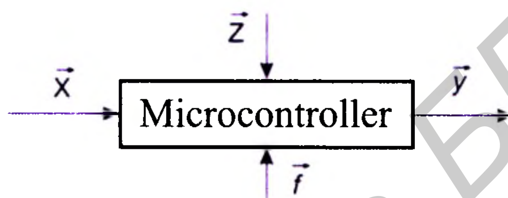

Figure 3.1. Schematic representation of a microcontroller for technical diagnostics

However, taking into account that the determining state of MC is the ability to perform the programmed functions, the operability condition of considered structural unit refers to the implementation of complex of the following inequalities (3.2) [2, p.16, equation 1.1]:

$$y_{j\min} \le y_j(x) \le y_{j\max}, \tag{3.2}$$

where $y_j(x)$ – function of operability;

$y_{j\max}$, $y_{j\min}$ – the maximum and the minimum value of j-th parameter.

Taking into account the fact that microcontrollers, on base of which most of the modern radioelectronic systems are built, have an increased rate of change of its parameters (analysis, processing and transmission of data, etc.) and also are quite sensitive to the impact of electrostatic discharges, this marks the task of providing the control of operability and searching the arising defects as one of the major.

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In this chapter the technique of determining the value of the voltage of static electricity discharge, at which occurs a change in the program code recorded into the built-in flash memory compared with the reference value of the data array, was developed and also this chapter proposes the method of functional control of microcontroller based on the experimental determination of the installation time of the code and on the calculating of operational failure rate.

To confirm the reliability of the developed methods of monitoring the functional and performance characteristics after the impact of electrostatic discharges the 8-bit microcontroller IN89C2051DW (manufacturer JSC «INTEGRAL») [23] was diagnosed.

This chapter represents the results of testing microcontrollers, which are the most common among manufacturers of modern electronic devices for various purposes.

3.1. Control of the functioning of microcontrollers after the impact of static electricity discharge

Control of the functionality of microcontrollers lies in the analysis of the quality of the performed functions, which depends on the quality of the data array recorded in built-in flash memory.

According to GOST 28195–89 [3], the quality of program code is determined by comparing the calculated values of parameters with the respective base values of parameters of the existing analogue or calculated code, taken as a reference sample.

The reference sample of the program code in the research includes all the programs, procedures, rules and associated documentation of the information processing system related to the functioning of microcontrollers, or a part of them.

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Taking into account the increased sensitivity of microcontrollers with the program code recorded into the built-in flash memory to the impact of electrostatic discharges and also the high probability of damage to the code, particular attention during the diagnostics should be paid to the data integrity.

The analysis of [3–6] reveals that the data integrity is a feature of data to save its structure and/or its contents during transmission and storage. The data integrity is provided in the case, when the recorded data doesn't differ from the data in the source documents, i.e. if there was no its accidental or intentional distortion or destruction.

The structure of most modern microcontrollers can be shown as a system of interconnected function units (FU), i.e. areas of MC chip, which organize the structure of the MC (see figure 1.). The objective of any FU is the strict execution of list of pre-programmed operations, correctness of execution of which can be controlled with the help of designed special test programs (TP) [7].

However, setting and formalization of problems of the estimating the impact of ESD on the change of program code recorded into the built-in flash memory of MC is significantly complicated by the fact that microcontrollers usually work under control of programs stored in its internal non-volatile memory, while for the storage of data being processed and for intermediate results microcontroller uses the internal random access memory. Limited access to these resources makes it more difficult to control the execution of the test programs needed for functional testing and detection of the failed blocks of modern MC.

It is also necessary to take into account a number of conditions for constructing the model of functional diagnostics of microcontrollers with built-in flash memory:

– if at least one FU of microcontroller is inoperative, then MC is considered to be inoperative;

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– for all diagnosable inputs and outputs of functional units of the microcontroller there are affordable limits of the parameters and if the parameter goes beyond these limits the microcontroller goes to the state of inoperability and is rejected;
– there is a program possibility of functional control of each tested FU of microcontroller.

When solving the problem of finding defects, state table (ST) is compiled using the following main provisions (table 3.1):

– informational data taken from all of the outputs of microcontroller are selected as the most important diagnostics parameters of MC ($Z_i = 0 - \infty$);
– informational data, which are acquired as a result of diagnostics, are a single system of test MC.

While compiling ST it is appropriate to use the number of columns corresponding to the number of direct diagnostic indicators and to the number of tests. Each line should contain the results of tests corresponding to the state of MC at the unacceptable reaction of one of FU.

At the same time, it is advisable to diagnose incorrect execution of programmed functions, that is identified in the operation of microcontrollers and caused by the impact of electrostatic discharge, with the help of specialized test programs (TP). These software tools are oriented at the detailed device structure and they can detect defects on the level of functional unit. The results of tests are presented in the state table of functional units, in which values of correct «1» or incorrect «0» execution of the test program are entered.

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Table 3.1. An example of the state table of functional units of microcontroller

Test program	Functional unit								
	FU1	**FU2**	**FU3**	**FU4**	**FU5**	**FU6**	**FU7**	**...**	**FU*n***
TP1	1	0	0	1	1	1	0	...	0
TP2	1	0	1	0	1	0	1	...	0
...	...	...	...	...	...	...	...	...	...
TP*n*	...	...	...	...	...	...	...	...	...
Result of test	1	0	0	0	1	0	0	...	0

The analysis of the results, obtained during the experiment, allows to make the conclusion on the feasibility of the search procedure of inoperative FU. If the malfunction is detected, then one can compile an algorithm for finding defects to a specific element included into the composition of microcontroller's chip. Thus, the algorithm must distinguish every pair of defects, i.e. the results of elementary tests included into the algorithm must be different in every inoperable state.

Number of lines in table 3.1 is defined combinotorially and is equal to the number of pairs of combinations of inoperable states [2, p. 95]:

$$M_l = C_Q^2, \tag{3.3}$$

where Q – number of inoperable states.

The analysis of formula (3.3) includes determination the minimum possible number of columns, at imposing of which a logical sum of each row is equal to one. This will allow to determine the minimum set of different tests, which is sufficient to detect a faulty or damaged FU. The results of tests for all states of tested microcontrollers are compared pairwise. The comparison results are entered into the additional table – confirmation table (table 3.2), in which in each line stands «+» if the test gave equal results or «-» if the test gave different results.

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Table 3.2. An example of the state table of functional units of microcontroller at re-testing

Test program	Functional unit								
	FU1	**FU2**	**FU3**	**FU4**	**FU5**	**FU6**	**FU7**	**...**	**FU*n***
TP1	+	-	-	+	+	+	-	...	-
TP2	+	-	+	-	+	-	+	...	-
...	...	...	...	...	...	...	...	...	...
TP*n*	...	...	...	...	...	...	...	...	...
Result of test	+	-	-	-	+	-	-	...	-

However, there are tests that in addition to the regular serial set of resolution have differences, which duplicate some of the results of previous tests. In this case, one of the duplicate tests can be eliminated, but only that, which is in addition to the main sequence of functions performs quite complete testing of others.

Today the most commonly used algorithm of functional testing for finding defects in the structure of microcontroller with the identification of certain damaged FU has the following sequence:

– on the basis of analysis of functions executed by microcontroller building of its unique functional structure with the specific highlight of its FU is carried out;
– the state table of FU is compiled;
– the state table of functional units of microcontroller is analysed and the minimum distinguishing set of results of state of FU is determined;
– sequence of execution of functional test for each separate function unit of microcontroller is ordered;
– parameters of diagnosis and acceptable limits of their changes are defined;
– algorithm for defect detection is constructed based on the results of the analysis.

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Thus, a general algorithm for testing of functional units of modern microcontrollers with built-in flash memory before the impact of static electricity discharge can be represented in the following way (figure 3.2).

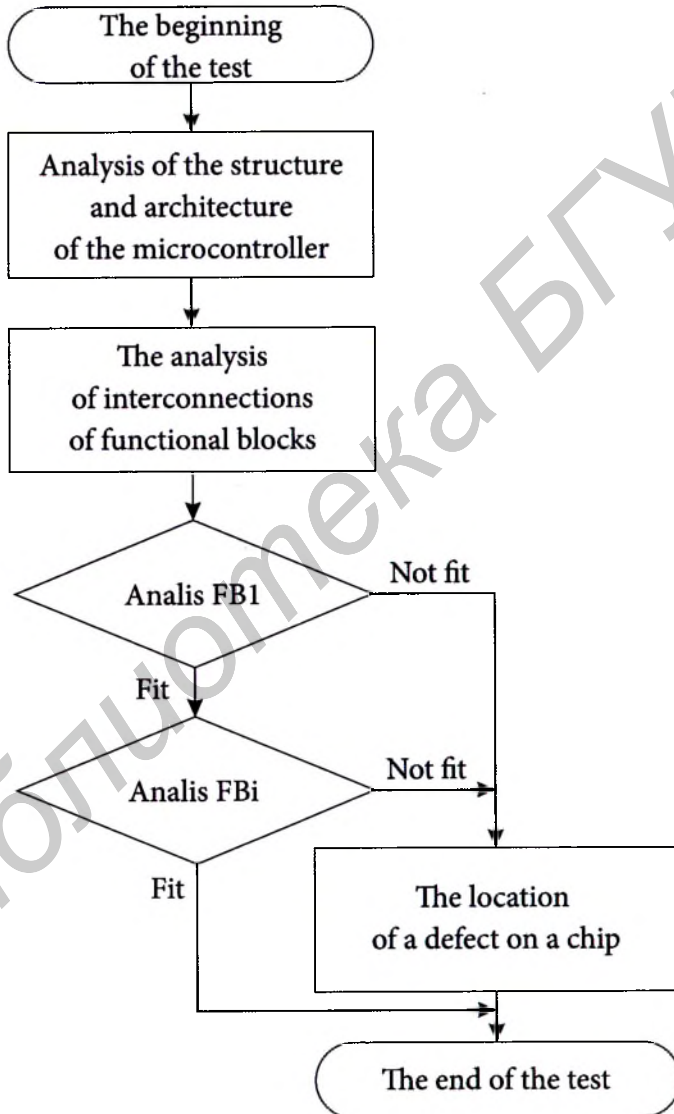

Figure 3.2. Algorithm for testing of functional units of microcontroller before the impact of static electricity

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When searching for multiple defects in this algorithm, faultfinding process is applied repeatedly with the required intermediate recovery, i.e. after a defect is found the searching process stops and locks, or an algorithm of testing of functional units finishes.

The above given algorithm can identify obvious damage (see p.1.5) of certain functional unit organized on a semiconductor chip of microcontroller or on its current-carrying elements. However, this algorithm does not allow to analyse changes in the program code of any complexity recorded into the built-in flash memory of MC.

3.2. Methods of analysis of microcontroller operability taking into account control of the state of program code recorded into the built-in flash memory after the contact impact of static electricity discharge

Testing microcontrollers with program code recorded into the built-in flash memory for determining an unstable operation in conditions of impact of static electricity discharge by the «human body model» is optimally performed on the basis of the six following steps (figure 3.3):

1. Formation of microcontrollers batches with the equal number of pieces in each.

Basic requirements for microcontrollers, which are a part of formed batch, are based on the rules presented in GOST 18725–83 [8]. At this stage close attention is paid to the appearance (scratches, cracks, change in geometry and in configuration of external pins, etc.), tightness of the housing, labeling, etc.

This item is caused by the fact that a set of hardware and a set of executed functions make modern MC with the built-in flash memory an effective mean of gathering, processing of information and of controlling objects. These features

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make microcontrollers from different manufacturers unique functionally complex devices, which have specific structure and architecture of the processor core. Thus, at this stage close attention is paid to the information provided in engineering specifications (ES) or in DataSheet.

2. Measurement of electrical parameters of microcontrollers before the impact of static electricity discharges.

For measuring electrical parameters of MC it is advisable to use digital storage oscilloscope, which allows to measure and to observe signals on ports of integrated circuits before and after the impact of static electricity. One of the recommended conditions is that the oscilloscope should record and display complex waveforms, random events and subtle features in the behavior of signals in real time and should provide information about signal in three measures: amplitude, time and the dependence of amplitude from time.

On this step the main point is to analyse the electrical parameters for compliance with those presented in ES or DataSheet. If information on the tested microcontrollers is not represented, the main guiding document for the implementation of the analysis of the electrical parameters is GOST 18725–83 [8].

3. The analysis of the program code recorded into the built-in flash memory of microcontroller before the contact impact of static electricity discharge.

For the analysis of the program code recorded into the built-in flash memory of microcontroller it is recommended to use a personal computer with universal programmer-tester connected, which is designed to program a wide range of modern MC. To eliminate any overlap of data array it is necessary to erase the flash memory of microcontroller, then the reference program code provided by the developer is installed into it. To confirm the correctness of done earlier operations (erase and record of the reference program code into the built-in flash memory of MC), reconciliation of the recorded data array with its reference value is carried out.

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4. Implementation of the contact impact of static electricity discharge on ports of microcontroller with the location of the discharge tip of the test generator of electrostatic discharges perpendicular to the external pin of microcontroller.

Execution of this item is caused by the need of improving the accuracy of the conducted tests, which is confirmed by the claims submitted in [9].

5. The analysis of the program code recorded into the built-in flash memory of microcontroller after the contact impact of static electricity discharge.

Main values of the electrostatic discharge voltage are given in [10]. In case of changes in the program code recorded into the built-in flash memory of microcontroller, voltage of static electricity discharge is recorded.

The algorithm shown on figure 3.3 implements a number of cycles, which allows to diagnose MC more adequately. Interval of increasing of voltage of static electricity discharge is chosen directly by the operator carrying out tests and it is also influenced by the specificity of the test equipment.

The main requirements for carrying out the experiments were the following:

– model of the discharge impact – «human body model»;
– discharge type – contact;
– number of discharges – 5 of each polarity;
– polarity – positive or negative;
– area of impact – external pin, which is responsible for operations of input – output of data;
– test generator – ESD3000 [24];
– analysis functions of data array (hash-functions) – MD5 and SHA1.

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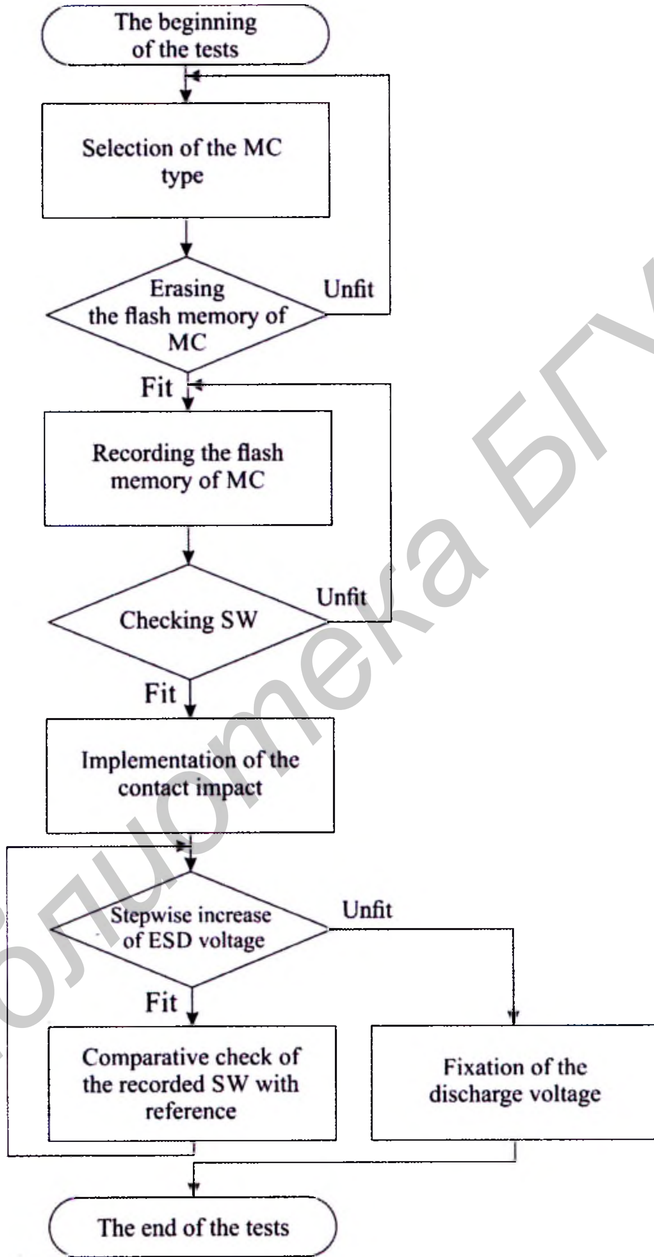

Figure 3.3. The algorithm for determining the voltage, at which the incorrect activation of programmed functions of MC with the BFM occurs, after the contact impact of SED

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Testing of MC for the resistance to ESD was carried out in laboratory conditions. The stand, designed in accordance with the requirements of STB IEC61000–4–2–2006 [36], consists of a test generator (TG), test equipment and auxiliary equipment necessary for implementation of impact with contact discharges (figure 3.4).

The stand for testing consists of a wooden table of 0,8 m in height, placed on a reference earthing plate, which is placed on the floor and represents a sheet 0,3 mm thick.

When testing MC for the resistance to the contact impact of static electricity it is the most optimal to use the test generator, designed for generating a normalized pulses for testing integrated circuits, that may be impacted by discharges.

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Figure 3.4. Appearance of the facility for testing microcontrollers for the resistance to static electricity impact by the method of contact discharge

Simplified scheme of the TG, simulating the static electricity discharge from the human body, is shown on figure 3.5 [36].

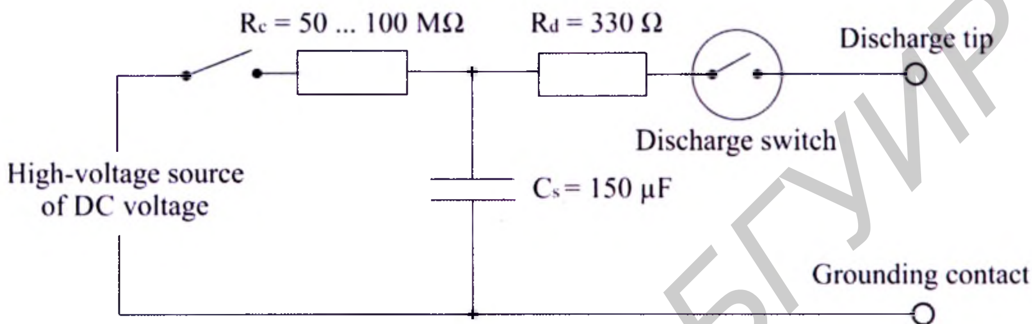

Figure 3.5. Scheme of the test generator, simulating the static electricity discharge from the human body

Technical parameters of the elements used in the scheme of facilities simulating the contact impact of discharge on the HBM must strictly conform to the values given in the table 3.3 [36]. A distinctive feature of the TG, simulating the contact impact of static electricity discharge, is that the discharge switch is always closed.

Table 3.3. Technical parameters of test generators [36]

Technical parameters	Value
Storage capacitor (*C*s)	150 pF ± 10%
Discharge resistance (*R*d)	330 Ω ± 10%
Charge resistance (*R*c)	from 50 to 100 MΩ
Output voltage	up to 15 kV
The indication error of the output voltage	± 5%
Polarity of the output voltage	Positive or negative
Hold time of the charge	Not less than 5 s
Discharge type	Single discharge (time between successive discharges not less than 1 s)

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To implement the contact electrostatic discharge, test generator is equipped with a special tip of the discharge electrode, the shape of which is shown on figure 3.6 [36]. The feature of the impact implementation is that at the contact discharge one should first touch the point of discharge, which is located on the external pin of the microcontroller, by the electrode tip and then turn on (close) the discharge switch of TG.

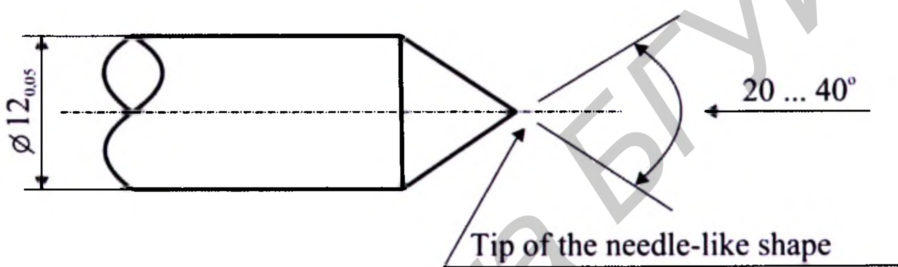

Figure 3.6. The shape of the discharge tip of the test generator for simulating the contact electrostatic discharge

Implementation of the mandatory requirements during the tests of modern MC for the resistance to the contact impact of static electricity discharge is necessary for an adequate evaluation of the experiment results.

The discharge tip of the test generator for the implementation of the static electricity contact discharge should be placed perpendicularly to the surface of the external pin of MC, as this will improve the repeatability of the test results.

In the tests of microcontrollers for the resistance to the contact impact of static electricity discharge on the HBM, the test generator must provide the following output pulse voltages (table 3.4) [39].

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Table 3.4. Parameters of the discharge current pulse from the body of operator [39]

Source voltage U, V	Peak current at the closure $1/I_{ps}$, A	Peak current in the resistor $R2$ I_{pr}, A	Rise time of the pulse t_r, ns	Rise time of the pulse through $R2$ t_{rr}, ns	Fall time at the closure t_d, ns	Decay current I_r, A
250	from 0,15 to 0,19	Not required	from 2,0 to 10	Not required	from 130 to 70	15% of I_{ps}
500	from 0,30 to 0,37	Not required	from 2,0 to 10	Not required	from 130 to 70	15% of I_{ps}
1000	from 0,60 to 0,74	from 0,37 to 0,65	from 2,0 to 10	–	from 130 to 70	15% of I_{ps} and I_{pr}
2000	from 1,2 to 1,48	Not required	from 2,0 to 10	Not required	from 130 to 70	15% of I_{ps}
4000	from 2,40 to 2,96	from 1,5 to 2,24	from 2,0 to 10	–	from 130 to 70	15% of I_{ps} and I_{pr}
8000 (additionally)	from 4,80 to 5,86	Not required	from 2,0 to 10	Not required	from 130 to 70	15% of I_{ps}

In case of testing microcontrollers for the resistance to the contact impact of electrostatic discharges regulated parameters of the test generator are used or requirements for the form of the current pulse are set. Consequently, compliance with the requirements, which lies in the need of matching with the parameters of acting discharge, presented in table 3.4, is mandatory for testing. In case of mismatch the results will have a high accuracy that will prevent getting the required one of conducted tests.

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3.3. Method of functional control of microcontrollers taking into account the changes of time of recording the code into the built-in flash memory after the contact impact of static electricity discharge

Due to the specifics of carrying out tests of microcontrollers with the program code of any complexity recorded into the built-in flash memory to the contact impact of static electricity discharge the method of functional control of microcontrollers was introduced. It consists of three stages: preparational, experimental and analytical (figure 3.7).

The main purpose of «preparation» stage is to identify potentially unreliable devices. This is done by defying the rejection criterias, by carrying out rejection tests, as well as by the analysis of the built-in flash memory taking into account the specificity of processes of erasing, recording and initialization of program code.

On the «experiment» stage the voltage, at which performance of microcontroller degrades, is determined with the determination of the degree of damage to the recorded data array.

On the «analysis» stage the analysis of reliability of the results and the formation of groups on the reliability of microcontrollers is carried out. It is executed by conducting the repeating test, which revealed the damage (degradation) of quality of performance of programmed functions. Also at this stage the calculation of operational failure rate of microcontrollers in conditions of impact of static electricity discharges is carried out.

Let us review the above listed stages more detailed with the description of algorithms and testing cycles.

«Preparation» stage helps to identify potentially unreliable microcontrollers and that increases the purity of conducted tests.

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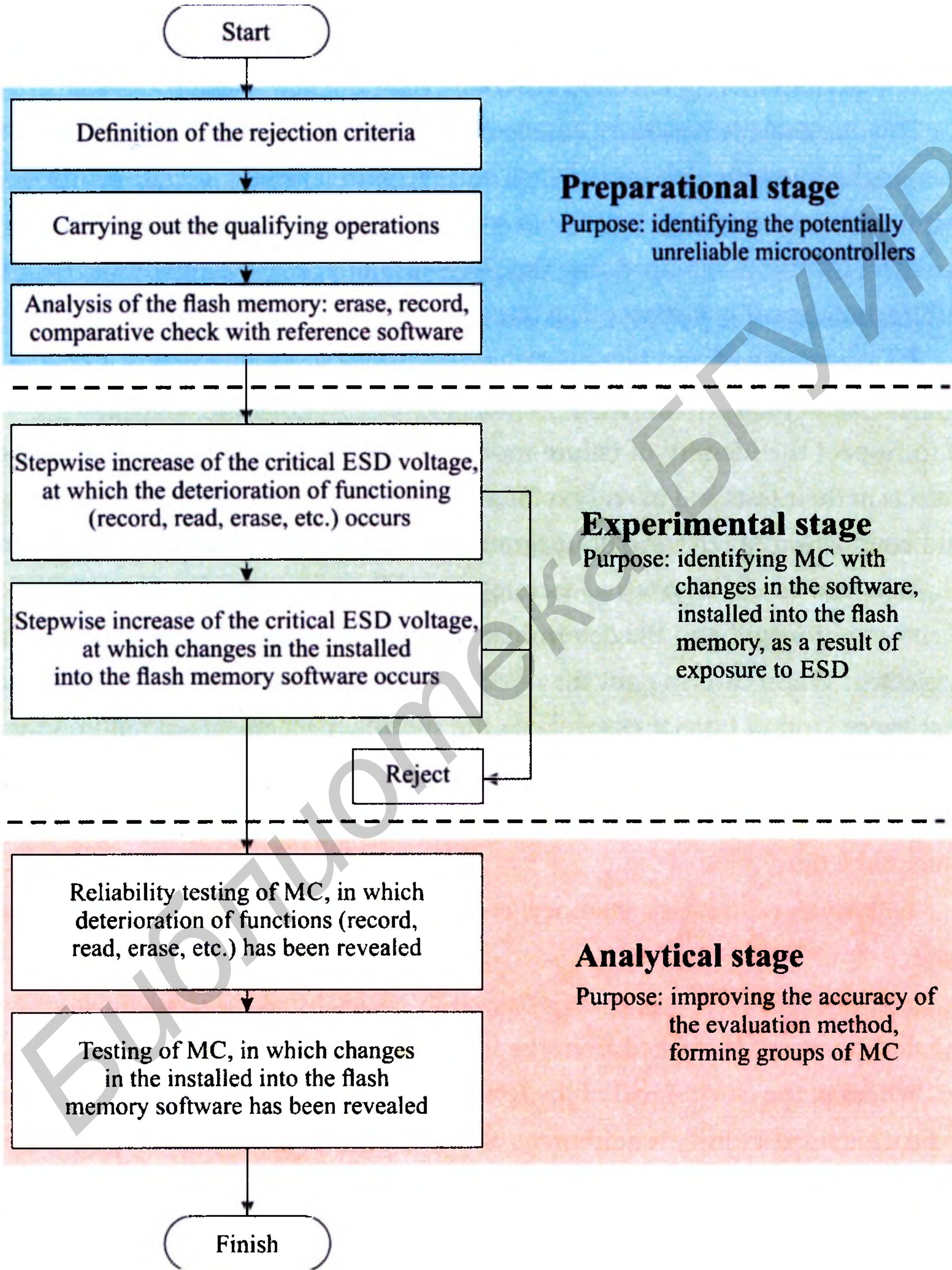

Figure 3.7. Algorithm of functional control of MC taking into account the changes of PC recording time into the BFM after contact impact of SED

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To do this, one must implement three following programs:

1. Determination of rejection criteria.

This program is necessary to ensure that the developer of MC during the tests highlighted the parameters that must remain constant after the impact of static electricity discharge on the external pin of the integrated circuit. These parameters include mean operating time between failures, mean operating time to failure, number of rewriting cycles, etc.

2. Conducting of rejection operations.

The main requirement to the regimes and conditions for rejections of MC is to respect the identity of failure modes and mechanisms of developments of defects in their tests and in real exploitation. Solving the problem of organization and conduction of rejection of integrated circuits involves selection of the composition and levels of external factors, to which the test specimens, modes of their operation and also the determination of the duration of training should be subjected. While carrying out the rejection one should pay attention to the fact that every kind of impact «provoked» the specific mechanisms of failure inherent to the test microcontrollers and their components, and diagnostical control should allow to detect these mechanisms in the early stages as a precursors to potential failures.

3. Analysis of the flash memory: erase, record and initialization of program code.

Introduction of this program is caused by the fact that the clock generator of the flash memory is clocked from the internal components of the microcontroller. Wherein, the clock signal of the selected source should be divided by the bits to provide the necessary requirements for the frequency. If a frequency deviation from the desired value during record or erase appears, the result of record or erase can be unpredictable, or the flash memory will be subjected to shock overload beyond the allowable limits, which ensure reliable work:

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1) process of erasing the flash memory of microcontrollers.

Preliminary erase of the built-in flash memory of microcontrollers is necessary for minimizing possible overlaps of installation code. While carrying out this process, clocking is conducted by the controller of flash memory and the central processor is stopped until the completion of the erase cycle. After the end of the erase cycle, central processor continues the execution of program from the command, which follows after the conducted record.

The sequence of the data erase from the built-in flash memory of MC can be represented as the following:

– load to the index of MC the address of erase block;
– set bit for selection of the flash memory program;
– set bit for record permission;
– set bit for erase permission;
– disable interrupts;
– set bit for the initialization of erase cycle;
– the central processor unit will stop execution of the program until the completion of the erase cycle;
– enable interrupts;

2) the process of installation data into the built-in flash memory of MC should be carried out in the following order:

– execution of erasing of the page;
– getting an address of the new page;
– filling the page buffers;
– recording of the page;

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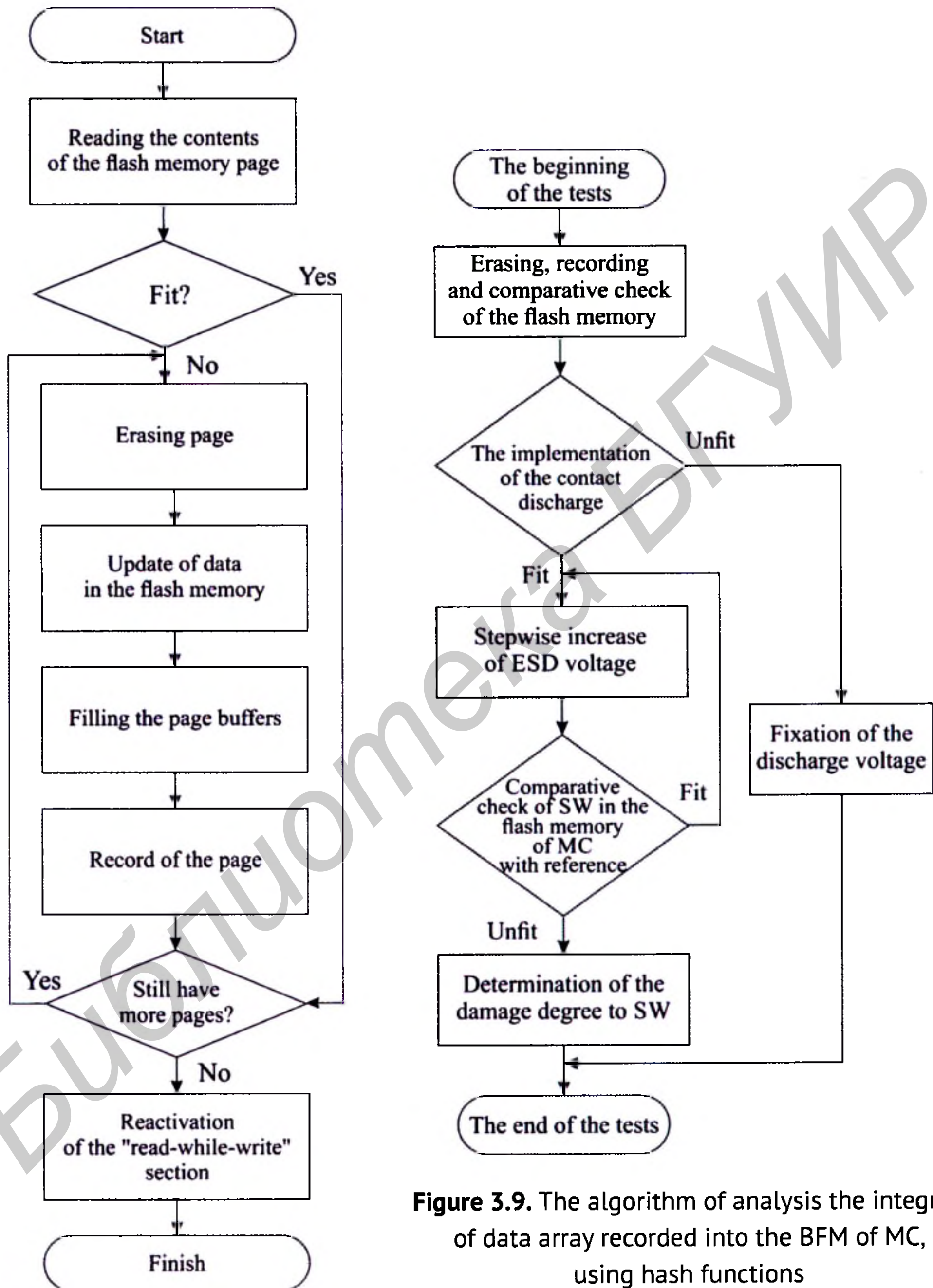

Figure 3.8. Initialization algorithm of PC recorded into the BFM of MC

Figure 3.9. The algorithm of analysis the integrity of data array recorded into the BFM of MC, using hash functions

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3) the initialization process of recorded program code of various complexity into the built-in flash memory of microcontroller is shown on figure 3.8.

The main objective of this paragraph is to implement a complete verification of compliance of program code recorded into the built-in flash memory of the microcontroller with its reference value, which is set by the developer (programmer) or other expert.

As a result of fulfilling all the above listed items of analytical stage the further research of microcontrollers with program code recorded in the memory takes place.

On the «experiment» stage an experiment on the contact impact of static electricity discharge at different voltages to the external pin of the microcontroller is conducted and the analysis of this impacts consequences is carried out.

The algorithm of stepwise increasing of the electrostatic discharge voltage, at which deterioration in the functioning of integrated circuits is detected, is shown on figure 3.9.

It should be considered that this algorithm is constructed using a number of cycles, which provide more accurate definition of integrity of program code recorded into the built-in flash memory.

It is advisable to perform the resistance test of microcontroller to the contact impact of static electricity discharge taking into account the following operations:

– working (operating) conditions of MC;
– test conditions of MC;
– points, to which the discharges should be applied;
– designation about what discharge (voltage, pulse duration, etc.) should be applied to each point;

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– testing level;
– number of discharges that should be applied to each point for the complete implementation of the test;
– the need for testing in a laboratory or at operational location.

The test program and software should ensure the implementation of the main operating modes by the test equipment. Using these means is allowed in cases when it is necessary to establish the correctness of MC functioning.

Test results are classified under conditions of loss of function or change in performance of microcontroller with program code recorded into the built-in flash memory with respect to certain performance criteria established by manufacturer. The following should be taken into account:

– normal functioning within the limits specified by the manufacturer, applicant or consumer;
– temporary reduction of the operation quality or loss of operability, the correction of which requires operator's intervention;
– temporary reduction of the operation quality or loss of operability, which stops after the impact of the disturbance and do not require operators intervention;
– decrease of the operation quality or loss of operability, which can not be recovered because of the damage to the components or data loss.

The analysis of the integrity of program code recorded into the built-in flash memory of microcontroller is carried out using such hash functions as MD5 (MessageDigset 5) and SHA-1 (SecureHashAlgorithm 1) [1–13]. The principle of forming a hash code is provided in Appendix D.

MD5 hash function is a 128-bit hash algorithm, which is designed to create «imprints» or «digests» of arbitrary length messages, i.e., using this function one

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can check correctness of recorded file. If the checksum established by the manufacturer (L) coincide, then the file was recorded without errors. The principle of this hash function operation is based on five steps.

The principle of SHA-1 code operation is that at the input message of arbitrary length the algorithm generates a unique 160-bit hash value. Base steps in the formation of a unique code SHA-1 are adding of the missing bits, adding the length, initialization of the SHA-1 buffer, processing of messages in 512-bit (16-word) blocks and output.

The additional use of such a cryptographic hash algorithm as SHA-1 will improve the efficiency of detection of changes in program code recorded into the built-in flash memory of microcontroller.

On the «analysis» stage the analysis of the reliability of conducted tests of MC and the assessment of their reliability after the impact of static electricity discharge is carried out.

Based on the fact that nowadays the vast majority of electronic devices is based on the principle of miniaturization, (so far) the most part of them contain microcontrollers, which according to the production technology can be classified as very large-scale integrated circuits (VLSIC). Moreover, they often play a key role in hardware, so the failure of one or another integrated circuit leads to the inevitable failure of the entire device. Getting an accurate assessment of MC reliability is necessary for calculating the reliability of the whole radioelectronic device. Therefore it is necessary to use adequate mathematical models for calculating reliability of each electroradioelement.

To develop the test programs (TP), we need to give a detailed review on each functional unit (FU), on basis of which one or the other microcontroller is designed.

According to [160], a functional unit (cell) refers to a set of elements of the MC base chip, which are electrically connected within one or more basic cells for implementation of one or more separate functions.

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Originally, microcontrollers, which were tested for the resistance to the impact of static electricity discharges, were presented as an interconnection between three main functional sectors: processor core, internal memory and peripherals and service modules.

Further partition was carried out taking into account the performed functions (table 3.5).

Table 3.5. Description of the functional units of microcontrollers, on which the contact impact of static electricity discharges was implemented

FU №	FU name	Description	Note
FU1	Instruction fetch and decode unit	Program counter PC	Processor core
FU2	State monitoring and execution of branching unit	Status register SR	
FU3	Subroutine call and implementation of the stack unit	Stack pointer SP	
FU4	Interruption implementation unit		
FU5	Operand address formation unit		
FU6	Arithmetic logic unit		
FU7	Operand shifter		
FU8	Multiplication-division unit		
FU9	Bit operations unit		
FU10	Register unit		Internal memory
FU11	Internal data RAM		
FU12	Internal memory of programs	Flash memory	
FU13	Interface with the external memory unit		Peripherals and service modules
FU14 … n	Input-output ports, timers, ADC, etc.		

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However, it should be noted, that microcontrollers used in the experiments for the resistance to the impact of static electricity discharges have a number of inaccessible for direct testing functional blocks (instruction register, data pointer).

At the same time, the structure does not have some important FU in explicit form such as operand address formation unit, operand shifter, interruption unit.

To test all the functional units included in the test microcontrollers, a set of test programs in Assembly language, which uses a basic list of necessary instructions executable by the processor, was developed.

The developed set of test programs provides the following sequence of testing the functional units as part of the microcontrollers tested for the resistance to the contact impact of static electricity discharges (table 3.6).

To install the TP into the built-in flash memory of the microcontroller it is required to apply a programing voltage of 12 V, and almost all port lines are used for control. Therefore, the process of flash memory programming is performed on specialized chip programmer of ROM – ChipProg [25].

For the integrity of experiments (absence of any external destabilizing impacts, in particular, electromagnetic interferences, crosstalks, etc.) and provision of the sufficient completeness of functional diagnostics the whole set of test programs was saved on a personal computer, as well as application for managing the specialized chip programer (figure 3.10).

Obtained as a result of functional diagnostics, parameters of all tested microcontrollers with the program code recorded into the built-in flash memory were consistent with those given in the technical descriptions, provided by manufacturers in the following sources [164–166].

Carrying out the functional control of all tested MC with program code recorded into the built-in flash memory after the contact impact of static electricity discharge on its external pin, was conducted in strict accordance with the developed algorithms and techniques.

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Table 3.6. Sequence of testing the microcontrollers functional units

TP №	Test field	Functional unit №
TP1	Testing of input-output ports	FU1, FU2, FU5, FU9 – FU11, FU13 – FU15
TP2	Testing of accumulator register	FU1, FU2, FU5, FU9 – FU11, FU13 – FU15
TP3	Testing of accumulator expansion register	FU1, FU2, FU5, FU9 – FU11, FU13 – FU15
TP4	Testing of RAM	FU1, FU2, FU5, FU9 – FU11, FU13 – FU15
TP5	Testing of ALU	FU1, FU2, FU5, FU9 – FU11, FU13 – FU15
TP6	Testing of multiplication/ division unit	FU1, FU2, FU5, FU8, FU9 – FU11, FU13 – FU15
TP7	Testing of state monitoring and branching execution	FU1 – FU3, FU5, FU9 – FU11, FU13 – FU15
TP8	Testing of the bit operations execution	FU1, FU2, FU5, FU7, FU9 – FU11, FU13 – FU15
TP9	Testing of interruptions	FU1 – FU5, FU9 – FU11, FU13 – FU15
TP10	Testing of the timer unit	FU1 – FU5, FU9 – FU11, FU13 – FU18
TP11	Testing of the watchdog timer	FU1 – FU5, FU9 – FU11, FU13 – FU15, FU17 and FU19
TP12	Testing of the internal memory	FU1 – FU5, FU9 – FU15, FU17 and FU19

Under the impact of static electricity discharges on microcontroller the initial (250 V) and the subsequent (500 V, 1 kV, 2 kV, 4 kV) voltages of current pulse correspond to the values listed in the current standards of the Republic of Belarus. To get the more accurate value of voltage, at which the change of data array recorded into the built-in flash memory occurs, its increase was carried out from the next lowest of the above values with step of 100 V.

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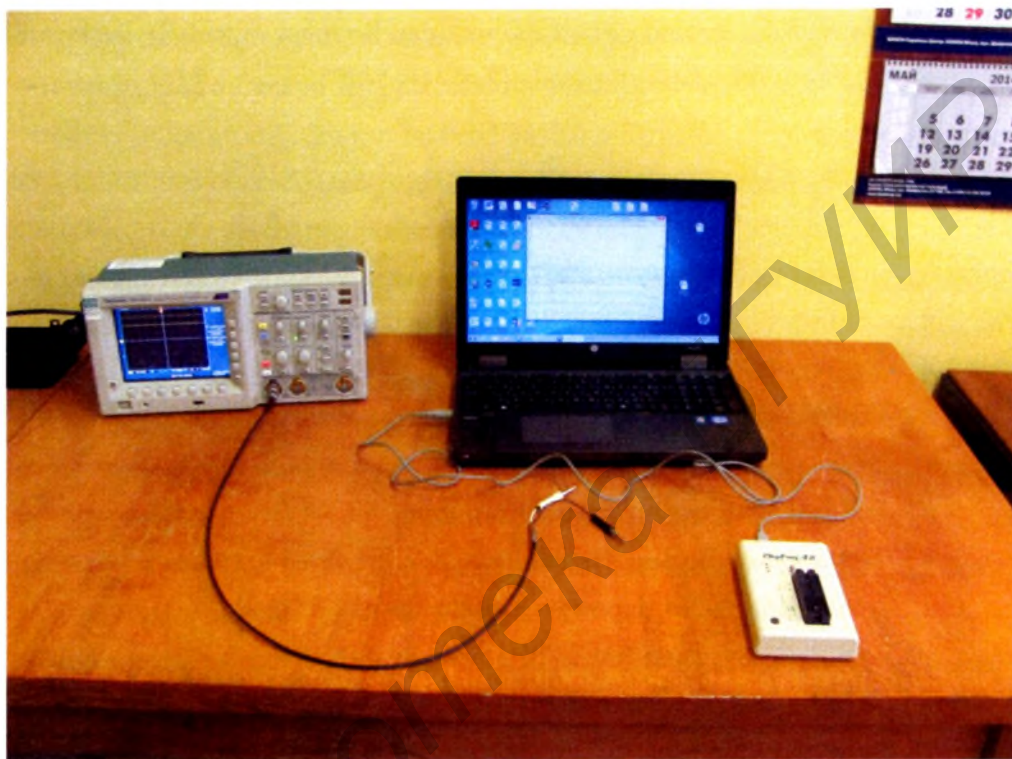

Figure 3.10. Appearance of the facility for the functional testing of microcontrollers after the impact of static electricity by the method of contact discharge

One of the main characteristics of trouble-free operation of semiconductor devices and electronic equipment, taking in account both sudden and gradual failures, that is given in technical documentation is operational failure rate λ_p [14, 15].

Based on the information presented in [14], in this study the operational failure rate of VLSIC is a conditional probability density of failure during the operation time of device, which is determined if that failure did not arise until the reported time.

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Let us review the principle of calculating the operational failure rate of very large-scale foreign integrated circuits, which can be most optimally performed using the following calculating formula (3.4) [15, 16]:

$$\lambda_P = (\lambda_{BD}\pi_{MGF}\pi_T\pi_{CD} + \lambda_{BP}\pi_E\pi_Q\pi_{PT} + \lambda_{EOS})\times 10^{-6}, \quad (3.4)$$

where λ_{BD} – failure rate of the die;

π_{MGF} – correction factor depending on the manufacturing process;

π_T – temperature mode factor;

π_{CD} – correction factor depending on the complexity of the die;

λ_{BP} – failure rate of the package;

π_E – factor depending on the environment;

π_Q – factor depending on the quality;

π_{PT} – correction factor depending on the type of package;

λ_{EOS} – failure rate depending on the voltage of ESD.

In the mathematical expression (3.4) the first summand describes the failure rate of the die, the second – the failure rate of the package, and the third (λ_{EOS}) – failure rate of fails due to the resistance of VLSIC to the impact of electrostatic discharge [15].

Cardinal difference of this model (3.4) from the existing mathematical models of calculating the operational failure rate is the presence of term λ_{EOS}, which is especially important for calculations of VLSIC that use CMOS technology which is the most sensitive to the impact of static electricity discharges [15, 17, 18].

The standard [16] provides the following formula for calculating λ_{EOS}:

$$\lambda_{EOS} = \frac{-\ln\left[1 - 0{,}00057\exp\left(-0{,}0002U_{TH}\right)\right]}{0{,}00876}\times 10^{-6}, \quad (3.5)$$

where U_{TH} – voltage of static electricity discharge, V.

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The analysis of the formula (3.5) shows that it does not take in account the impact type of discharge, namely contact or air.

Given in [16] values of λ_{EOS} are calculated only for contact impact of static electricity discharge and can not be used in the calculation of operational failure rate in conditions of air ESD impact. It is caused by the fact that during the spread of static electricity discharge in the gas medium it's fading.

In this regard, we transform the formula (3.5), by entering a correction factor K_{ESD}, which will take into consideration the type of static electricity discharge in the calculation of failure rate λ_{EOS}, into the following (3.6):

$$\lambda_{EOS} = \frac{-\ln\left[1-0{,}00057\exp\left(-0{,}0002K_{ESD}U_{TH}\right)\right]}{0{,}00876}\times 10^{-6}, \quad (3.6)$$

where K_{ESD} – correction factor, that takes into account the type of static electricity discharge impact (contact or air).

Based on the information presented in [19, 20], we calculated the values of coefficient K_{ESD} for the corresponding voltages and static electricity discharge type. The principle of calculation of this coefficient is in the maximum approximation of the voltage of air discharge to contact discharge, taking into account the conditions of the same degrees of tests rigidity.

Based on the listed above information, calculation of the correction factor (K_{ESD}), taking into account the type of static electricity discharge impact (contact or air) was carried out as follows (3.7):

$$K_{ESD} = \frac{U_{TH(\text{contact})}}{U_{TH(\text{air})}}, \quad (3.7)$$

where $U_{TH\,(contact)}$ – voltage of contact static electricity discharge, V.

$U_{TH\,(air)}$ – voltage of air static electricity discharge, V.

Values of the correction factor obtained by calculation using the formula (3.7) are shown in table 3.7.

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Table 3.7. Values of the correction factor K_{ESD} taking into account the type of static electricity discharge and its voltage

Degree of tests rigidity	Contact ESD		Air ESD	
	Voltage $U_{TH\ (contact)}$, V	Coefficient K_{ESD}	Voltage $U_{TH\ (air)}$, B	Coefficient K_{ESD}
1	2000	1	2000	1
2	4000	1	4000	1
3	6000	1	8000	0,75
4	8000	1	15000	0,53

Due to the fact that the introduced correction factor for the contact type ESD equals one (K_{ESD} = 1), regardless of the voltage level, the results of calculations with the introduction of coefficient will not differ from the results calculated using the formula (3.5).

In case of air impact of static electricity discharge on VLSIC with voltage 8000 V and 15000 V, the values of the operational failure rate should be calculated using the formula (3.6) with the introduction of correction factors of 0,75 and 0,53 respectively.

The difference between calculations of failure rate λ_{EOS} with and without the correction factor, at different voltages of impacting static electricity discharge in the mandatory fulfillment of the condition of the same degrees of conducted tests rigidity, is presented on a comparative graph (figure 3.11).

The graph shows that accuracy of calculation of failure rate value (λ_{EOS}), that takes into account the voltage of impacting static electricity discharge and its type, increases 1,5 times (at $U_{TH\ (air)}$ = 8000 V), and 4 times (at $U_{TH\ (air)}$ = 15000 V).

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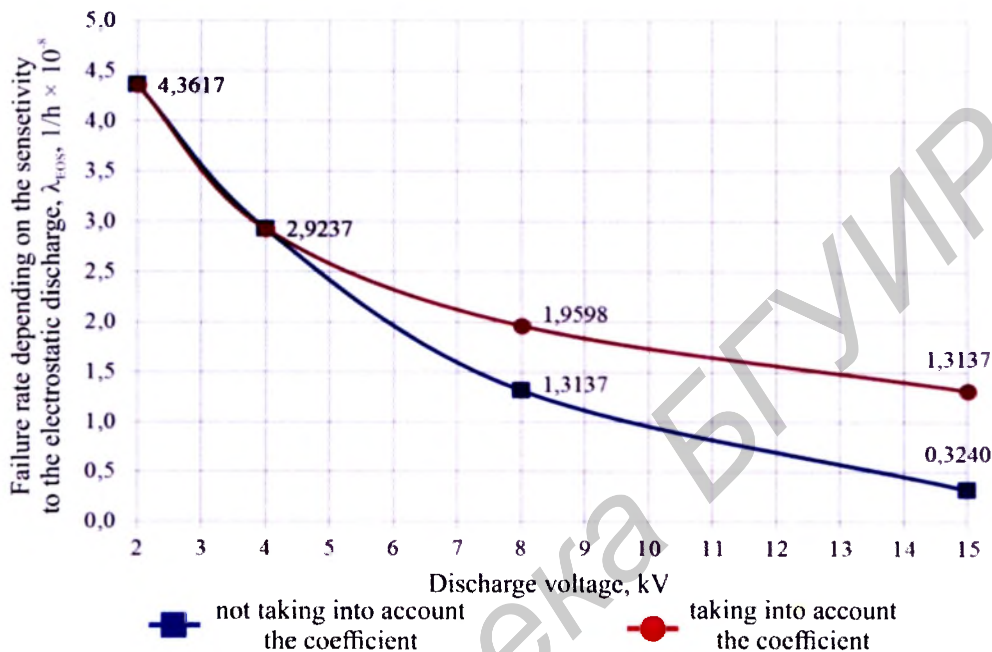

Figure 3.11. Graph of comparing the calculation of failure rates in the respective voltages of static electricity discharge

Thus, it was experimentally found that using of mathematical model (3.5) in air impact of static electricity discharge leads to incorrect calculation of the value λ_{EOS}. It was shown that introduction of the correction factor K_{ESD} allows to correct the calculation and get the most accurate result.

To confirm the effectiveness of the correction factor introduction into the calculation of the failure rate, which depend on the voltage of ESD, we perform the calculation of the operational failure rate (λ_p) of VLSIC type IN80C49N (manufacturer JSC «INTEGRAL» – holding management company «INTEGRAL»). This integrated circuit is a high-performance single-chip 8-bit microcontroller, based on CMOS technology of high density, and it is designed for use in household appliances, communications, technological and transport process control

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systems and in other areas of national economy [21], which emphasizes its demand in the production of not only domestic, but also foreign devices. In this regard, the calculation was performed using the mathematical model (3.4).

In calculations we used numerical values of parameters, which were received using the models and tables listed in [16, 21, 22], and also from reports on the reliability, which were obtained in the framework of the conducted researches on grant of the Ministry of Education of the Republic of Belarus (№ ГР 20121726).

Below is a graph comparing the calculation results (figure 3.12).

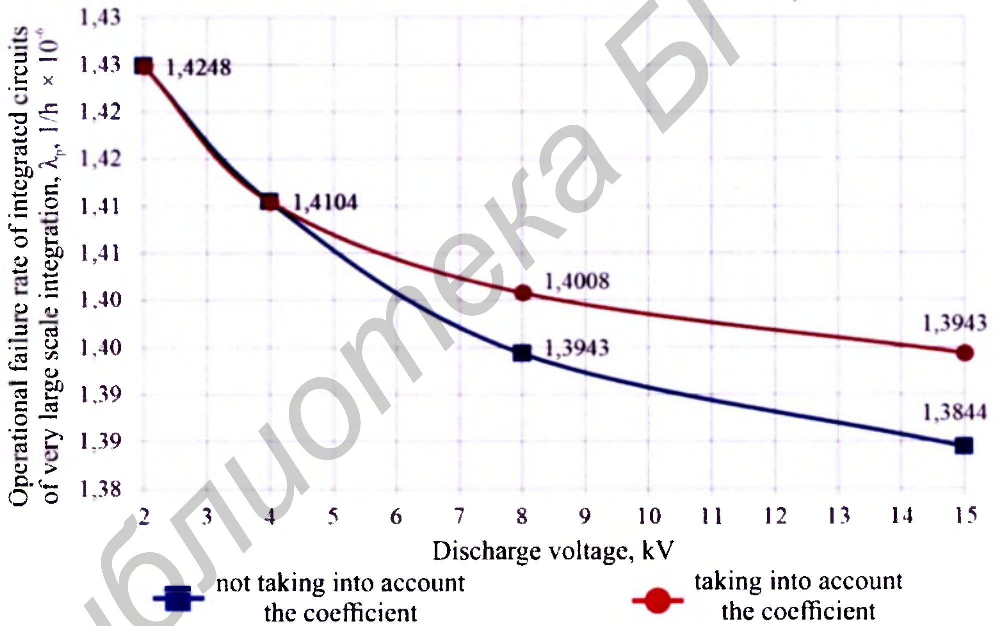

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Figure 3.12. Graph comparing the calculation of operational failure rate of VLSIC type IN80C49N for different types of impact of static electricity discharge

The results in figure 3.8 show that the accuracy of calculation of operational failure rate of VLSIC type IN80S49N at the impact of static electricity discharges, taking into account the correction factor, is higher. Thus, at the pulse discharge current voltage 8 000 V the accuracy is improved by 0,46%, and at 15 000 V – by 0,71%.

Conclusions of chapter 3

1. The algorithm controlling the functioning of MC after the impact of static electricity discharges was developed basing on the submission of test microcontroller by means of functional blocks. It was shown that the critical value of pulsed discharge affecting the external pin of microcontroller is not such an important indicator as the voltage at which occurs the disturbance of programmed functions. To determine the values of these voltages it is advisable to use stepwise ESD voltage increase on the condition that characteristics of impacting pulse discharge are the same.

2. It is shown that incorrect execution of programmed function of MC due to the impact of static electricity discharge is advisable to diagnose using specialized test programs, which are designed for a specific processor cores architecture of microcontroller. This will detect defects at level of particular functional block, not only in the system of current-carrying elements.

3. A method of analyzing the performance of microcontroller based on state control of the recorded code with stepwise increase of impacting electrostatic discharges voltage (step 0,1 kV), which provides the definition of the threshold value of discharge voltage (more than 75% of its limit) resulting in a change of code, was developed. The feature of this method is in identifying potentially unreliable MC with the analysis of the recorded code integrity using specialized test equipment (facility for testing microcontrollers for resistance to the impact of static electricity discharges, and also facilities for their functional testing).

4. A method of microcontrollers functional control based on the impact of static electricity discharges, that confirms the increase in the time of recording program code up to 16 times (at the discharge voltage up to 8 kV), was developed. This method allows to determine possible disturbances in the built-in flash memory of integrated circuits, which in its turn will ensure the prevention of false activation of systems designed on the basis of MC.

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5. A numerical model for calculation of the microcontrollers failure rate including the correction factor was developed, which takes into account the impact type (contact or air) and the voltage of static electricity discharge (for contact discharge a correction factor is equal to 1; for air discharge it is equal to 0,75 at the discharge voltage of 8 kV and to 0,5 at the discharge voltage of 15 kV), that can improve the accuracy of calculations up to 50% compared to the known models of reliability estimation.

5. The analysis of microcontroller IN89C2051DW using the developed test programs shows that disturbance in the program code recorded into the built-in flash memory occurs much earlier than catastrophic damage of the MC.

6. Voltages, at which the damage in the code recorded into the built-in flash memory of microcontroller occurs, were experimentally determined. For MC type IN89C2051DW it is over over 75% of the limit value of the discharge voltage. Then were determined voltages, at which functional and program (IN89C-2051DW – from 1,4 kV) disturbances in its operating occur.

6. Using specialized equipment, it was experimentally determined that at the voltage of static electricity discharge from 2 to 8 kV recording time of the code into the built-in flash memory of microcontroller increases from 2 to 16 times. It was established, that the change of the code record speed is associated with the disturbance of integrity of the flash memory functional cells.

7. Based on the adequate models for calculating the operational failure rate of integrated circuits taking into account the integration degree, there were experimentally obtained the values of the correction factor (K_{ESD}), which take into account the method of discharge impact:

– for the contact discharge of different voltages in tests of all degrees of hardness – $K_{ESD} = 1$;
– for air discharge at voltages 2 kV and 4 kV – $K_{ESD} = 1$;
– for air discharge at voltage 8 kV – $K_{ESD} = 0,75$
– for air discharge at voltage 15 kV – $K_{ESD} = 0,5$.

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Introduction of coefficients improves the accuracy of calculating the operational failure rate of microcontrollers with the built-in flash memory up to 50%.

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DEDUCTION

Main scientific results

1. The analysis of existing methods of monitoring functional and operational characteristics of microcontrollers for the resistance to static electricity discharges was performed. It was shown that the detection of changes in electrical (static and dynamic) parameters of microcontrollers is not the most important indicator, since the damage of program code recorded into the built-in flash memory is highly probable. The necessity of developing the new approaches to the technical diagnostics of microcontrollers with data array recorded into the built-in flash memory was justified [1–A, 2–A, 6–A, 11–A, 12–A].

2. A linear dependence of the temperature change in the system of current-carrying elements («external pin» – «traverse» – «contact pad» – «metallized track» – «semiconductor chip») of integrated circuits from the static electricity discharge voltage was established. It was experimentally found that due to the contact impact of electrostatic discharge on the external pin the change of temperature in the system of current-carrying elements is from 300 K (at a discharge voltage of 2 kV) to 430 K (at a discharge voltage of 8 kV). The difference between temperatures on the areas of contact «external pin – traverse» and «traverse – contact pad» was determined, which is in the range from 10 K (at a discharge voltage of 2 kV) to 140 K (at a discharge voltage of 8 kV) [5–A, 8–A, 9–A, 10–A, 13–A, 14–A].

3. The voltages, at which the code is damaged after the impact of static electricity discharges, were experimentally determined. For microcontrollers type IN-89C2051DW it is over 75% of the limit value of the discharge voltage. The values

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of voltage, at which functional and program (IN89C2051DW – from 1,4 kV) disturbances occur in operating of microcontrollers, were determined [3–A, 4–A].

4. Using the developed method of functional control of 8-bit microcontrollers with program code recorded into the built-in flash memory after the impact of static electricity discharges, an increase in the record time of the data array was revealed. It was experimentally established that at a discharge voltage from 2 to 8 kV, code record time is increased from 2 to 16 times. It was shown that the change of code installation speed is associated with the disturbance of the flash memory cells integrity [1–A, 2–A, 3–A, 4–A, 15–A].

5. It was found that the calculation of the microcontrollers' failure rate as a result of the impact of static electricity discharge is advisable to carry out taking into account the type of discharge (contact or air). It was shown that increasing of the calculation accuracy is possible by the introduction of correction factor (K_{ESD}), that takes into account the method of discharge impact, discharge current and voltage, and also the relative humidity of environment. As a result of calculation, the following values of the correction factors were obtained: for the contact discharge at different voltages – K_{ESD} = 1; for air discharge at U_{ESD} = 2 kV and U_{ESD} = 4 kV – K_{ESD} = 1; at U_{ESD} = 8 kV – K_{ESD} = 0,75 and at U_{ESD} = 15 kV – K_{ESD} = 0,5. Introduction of the proposed factor improves the accuracy of the failure rate calculation of microcontrollers with the built-in flash memory up to 50% compared with the known models of reliability estimation [7–A, 16–A].

Recommendations for practical use of the results

1. It was proposed to use the obtained linear dependencies of the temperature change in the system of current-carrying elements of microcontrollers for more adequate description of the thermal nonstationarity taking into account physical-chemical properties of each element as a result of the impact of electrostatic

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discharges. This will optimize technological processes in manufacturing, and also in development and introduction of promising materials for these elements [8–A, 9–A, 10–A].

2. The developed methods of technical diagnostics of functional and operational characteristics of microcontrollers with the built-in flash memory after the impact of static electricity discharge can be used in semiconductor industry in the implementation of design and development of modern integrated circuits (formation of protective structures, optimization of topological sizes, grading of potentially unreliable components, etc.) [15–A, 16–A].

3. Conducted series of experiments on the microcontrollers with program code recorded into the built-in flash memory for the resistance to the impact of electrostatic discharges confirms the reliability of the developed techniques. Obtained results are introduced on such industrial enterprises of the Republic of Belarus as JSC «KBTEM-OMO» and JSC «INTEGRAL» – holding management company «INTEGRAL».

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APPENDIX A

Main technical characteristics of various manufacturers' microcontrollers

Table A.1. Technical characteristics of modern 8-bit microcontrollers of foreign production [69–75, 77, 78, 80]

Manufacturer	Processor	Clock rate, *MHz*	Instructions' internal memory	Data internal memory	Peripheral units
Analog Devices	MCS-51, CISC	Up to 20	8, 32, 64 K	Up to 4 K	SPI, UART, 12C, WDT, DMA, DAC, ADC
Atmel	AVR, RISC	Up to 20	Up to 256 K	Up to 8 K	SPI, UART, 12C, WDT, ADC, RTC, AC, PWM, USB
	MCS-51, CISC	Up to 60	Up to 128 K	Up to 2 K	SPI, UART, 12C, WDT, ADC, USB
Freescale Semiconductor	CPU08-R, CISC	Up to 50	Up to 128 K	Up to 8 K	SPI, SCI, 12C, WDT, ADC, USB, CAN
	CPU08-S, CISC	Up to 20	Up to 60 K	Up to 4 K	SPI, SCI, 12C, WDT, ADC
Microchip Technology	PIC12, RISC	Up to 20	Up to 3584 K	Up to 128 K	WDT, ADC, AC
	PIC16, RISC	Up to 20	Up to 14 K	Up to 368 K	UART, WDT, ADC, AC, 12C, SPI, PWM, USB
	PIC18, RISC	Up to 64	Up to 128 K	Up to 3840 K	UART, 12C, WDT, ADC, AC, PWM, SPI, CAN
NXP Semiconductor	MCS-51, CISC	Up to 33	Up to 64 K	Up to 8 K	SPI, UART, 12C, WDT, ADC, RTC, PWM

Note. Table acronyms are the following: SPI – serial peripheral interface; WDT, RTC – watchdog timer and real time clock respectively; PWM – pulse-width modulator; DMA – direct-memory access controller; AC – analog comparator.

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Table A.2. Technical characteristics of modern 16-bit microcontrollers of foreign production [69–73, 81. 82]

Manufacturer	Proccessor	Clock rate, *MHz*	Instructions' internal memory	Data internal memory	Peripheral units
Renesas Technology	H8	Up to 25	Up to 512 K	Up to 16 K	SCI, 12C, WDT, ADC, DAC, USB, CAN
	H8S	Up to 33	Up to 256 K	Up to 32 K	UART, 12C, WDT, ADC, DAC, CAN, PWM, RTC
	M16C	Up to 20	Up to 256 K	Up to 20 K	UART, WDT, ADC, DAC, CAN, PWM, USB
	R8C	Up to 20	Up to 16 K	Up to 4 K	UART, WDT, ADC, DAC
STMicro-electronics	ST10	Up to 60	Up to 256 K	Up to 12 K	UART, WDT, ADC, CAN, PWM, SSC
Texas Instruments	MSP430	Up to 8	Up to 60 K	Up to 2 K	WDT, PWM, 12C, UART, ADC, DAC
Freescale Semiconductor	HCS12	Up to 50	Up to 512 K	Up to 14 K	WDT, PWM, SCI, SPI, 12C, USB, CAN, EN
Intel	MCS-96	Up to 50	Up to 32 K	Up to 1,5 K	PWM, UART, HSIO, EPA, CAN
Infineon Technolo-gies	C16	Up to 40	Up to 256 K	Up to 11 K	PWM, WDT, UART, ASC, 12C, PCM, USB, SSC, ADC, RTC

Note. Table acronyms are the following: ADC, DAC – analog to digital and digital to analog converter; EN – Ethernet network; HSIO – high-speed input-output module; SSC, ASC – synchronous and asynchronous serial channels; UART, SCI – universal asynchronous receiver/transmitter and serial communications interface.

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Table A.3. Technical characteristics of modern 32-bit microcontrollers of foreign production [69–74, 77, 78, 80, 82]

Manufacturer	Processor	Clock rate, *MHz*	Instructions' internal memory	Data internal memory	Peripheral units
Analog Devices	ADuC70 (ARM7TDMI)	Up to 45	62 K	8 Kbyte	PWM, UART, SPI, 12C, ADC, DAC, comparator
Atmel	AT91SAM7 (ARM7TDMI)	Up to 75	Up to 2048 K	Up to 256 K	USART, SPI, WDT, ADC, DAC, IrDA
	AT91SAM9 (ARM9)	Up to 180	Up to 2048 K	Up to 256 K	USART, SPI, WDT, ADC, DAC, IrDA
Freescale Semicon-ductor	MCF5xxx (ColdFire)	Up to 200	-	Up to 64 K	PWM, WDT, UART, CAN, 12C, USB, EN, ADC, DMA
	MCF5xxx, (PowerPC)	Up to 80	Up to 1024 K	Up to 36 K	PWM, CAN, SCI, QSPI, DMA
NXP Semicon-ductor	LPC2000 (ARM7TDMI)	Up to 60	Up to 512 K	Up to 40 K	PWM, UART, 12C, SPI, CAN, ADC, WDT, RTC
	LPC3180 (ARM9I)	Up to 200	-	64 K	UART, 12C, SPI, USB, DMA, ADC, MMU
Renesas Technology	SH-2, SH-3 (SH)	Up to 200	-	32 K	USART, 12C, SPI, CAN, WDT, EN, IrDA, RTC
Texas Instru-ments	MSP470 (ARM7TDMI)	Up to 60	1,25 M	Up to 80 K	SPI, SCI, 12C, CAN, ADC

Note. Table acronyms are the following: IrDA – infrared data association unit; USART – universal synchronous/asynchronous receiver/transmitter unit; MMU – memory management unit; 12C, USB, CAN – controllers of bus interfaces 12C, USB, CAN.

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APPENDIX B

Software and hardware complex for getting the digital images of damage to the current-carrying elements of integrated circuits after the contact impact of static electricity discharge

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Continuous growth of developed integrated circuits' complexity, as well as the global trend towards the submicron technologies require significant efforts to get the complex information about the materials used, microelectronic devices' parameters and other objects. Since the range of the researched materials is very wide, the complex of equipment must have an opportunity to analyse the wide set of physical parameters and have an opportunity, if it is necessary, to obtain the needed information quickly and reliably.

In photomicrography of integrated circuits' failures, caused by the impact of electrostatic discharges, software and hardware complex for getting the digital images, located in the state center «Belmicroanalysis» (the branch of JSC «INTEGRAL» – holding managing company «INTEGRAL») (figure B.1) was used.

This complex includes:

1. Light microscope Leica INM100 (figure B.2).

2. Digital camera DS-Fi1 (figure B.3).

This camera has a 5-megapixel CCD matrix, which allows to obtain high-resolution images with size of 2560x1920 pixels, provides a high frame rate, improves resolution, widens dynamic range and suppresses noise.

3. Precision automated scanning table 200×200 mm with the control unit LSTEP13.

4. The graphic station.

5. UV-range attachment with zoom up to 6000x.

6. Printer HP Color LaserJet 2605.
7. Tripod for macroshooting (Copy Stand).

Figure B.1. Software and hardware complex for getting the digital images of damage to the current-carrying elements of integrated circuits

Figure B.2. General view of light microscope Leica INM100

Figure B.3. General view of digital camera DS-Fi1 (Nikon)

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APPENDIX C

The results of modeling the thermal processes distribution in the system of integrated circuits' current-carrying elements due to the contact impact of static electricity discharge

C.1. The results of the thermal processes distribution in the area of the traverse maximum bending of integrated circuit after the contact impact of electrostatic discharge

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Figure C.1. Three-dimensional model of the current-carrying elements system of integrated circuit with designation of the most heat-loaded area of the traverse as a result of the impact of static electricity discharge

Figure C.2. Three-dimensional model of the maximum bending area of integrated circuits' traverse, in which the analysis of the thermal unsteadiness distribution is conducted as a result of the static electricity discharge impact

Table C.1. Numerical temperature values in the maximum bending area of integrated circuits' traverse

Test point	Distance between points, μ*m*	The temperature values (*K*) at the discharge voltage				
		2 kV	4 kV	6 kV	8 kV	15 kV
1	0	294	300	305	320	371
2	250	296	316	347	382	625
3	500	299	318	353	387	636
4	750	301	318	353	388	638
5	900	305	337	395	498	1047
6	925	306	338	398	500	1076
7	950	306	340	390	500	1072
8	975	306	338	389	496	1049
9	1000	306	338	386	485	1042
10	1100	302	317	348	390	636

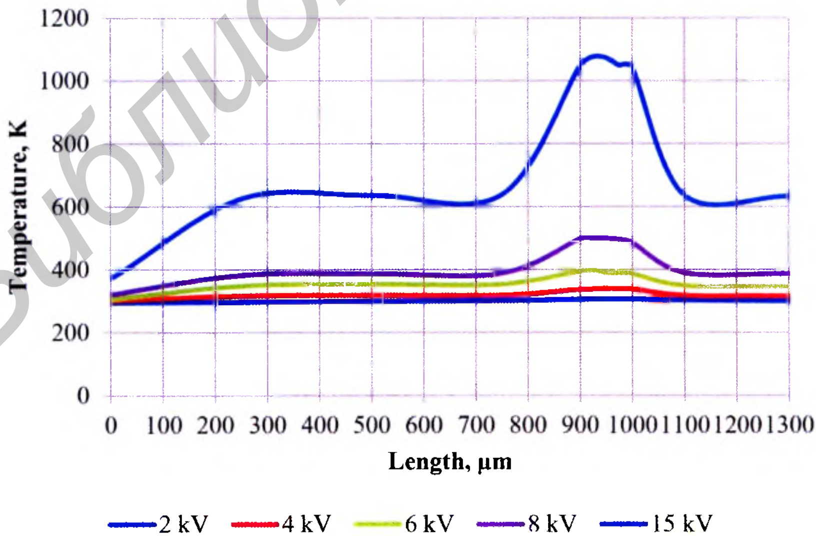

Figure C.3. The temperature distribution in the maximum bending area of IC traverse

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Table C.2. Numerical values of the electromagnetic losses power in the maximum bending area of the integrated circuits' traverse

Test poing	Distance between points, µm	Value of the electromagnetic losses power ($W/m^3 \times 10^{16}$) at the discharge voltage:				
		2 kV	4 kV	6 kV	8 kV	15 kV
1	0	0,057	0,38	0,45	1,6	2,24
2	250	0,383	1,52	3,52	6,49	14,63
3	500	0,391	1,56	3,61	6,54	14,82
4	750	0,524	1,63	3,64	6,71	14,86
5	900	0,631	3,49	8,584	14,6	29,31
6	925	0,591	3,51	8,732	15,1	30,41
7	950	0,581	3,26	8,421	14,8	30,22
8	975	0,576	3,24	8,392	14,7	29,84
9	1000	0,576	3,17	8,367	14,4	29,39
10	1100	0,361	1,65	3,52	6,49	14,25

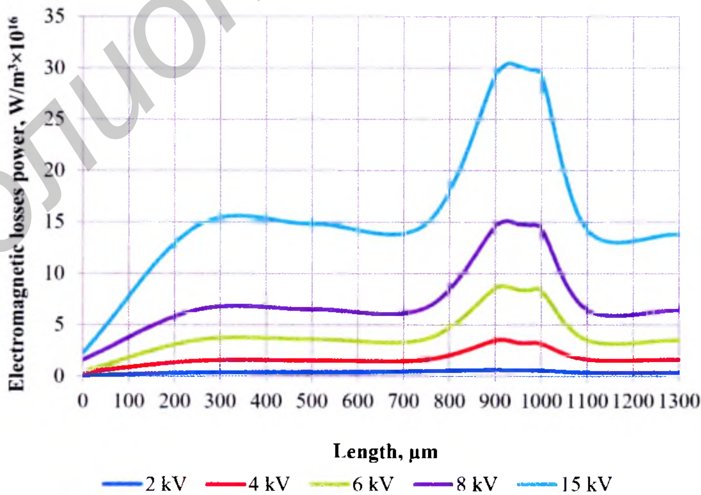

Figure C.4. The distribution of the electromagnetic losses power in the maximum bending area of IC traverse

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Table C.3. Numerical values of the electric field strength in the maximum bending area of integrated circuits' traverse

Test point	Distance between points, μ*m*	Values of the electric field strength (*W/m*) at the discharge voltage:				
		2 kV	4 kV	6 kV	8 kV	15 kV
1	0	2526	5064	12676	17145	23127
2	250	9103	18568	27660	37216	83142
3	500	9226	19042	28739	37420	84074
4	750	9301	19100	28800	37716	82321
5	900	12030	24381	34630	49122	102323
6	925	12430	25227	37424	51433	106354
7	950	13010	27000	39842	53242	110423
8	975	12700	26800	38138	52672	106234
9	1000	12626	26660	37230	51821	103112
10	1100	9489	18524	28533	38326	82132

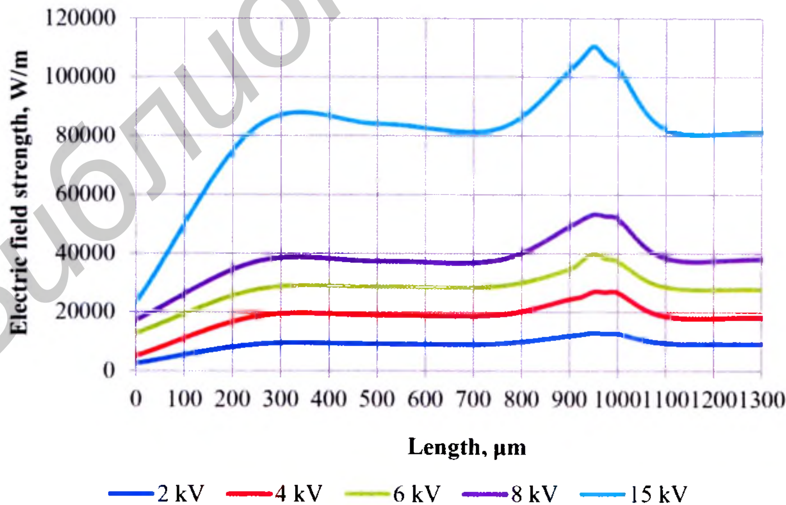

Figure C.5. The distribution of the electric field in the maximum bending area of IC traverse

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C.2. The results of thermal unsteadiness distribution in the system of integrated circuits' current-carrying elements after the contact impact of static electricity discharge

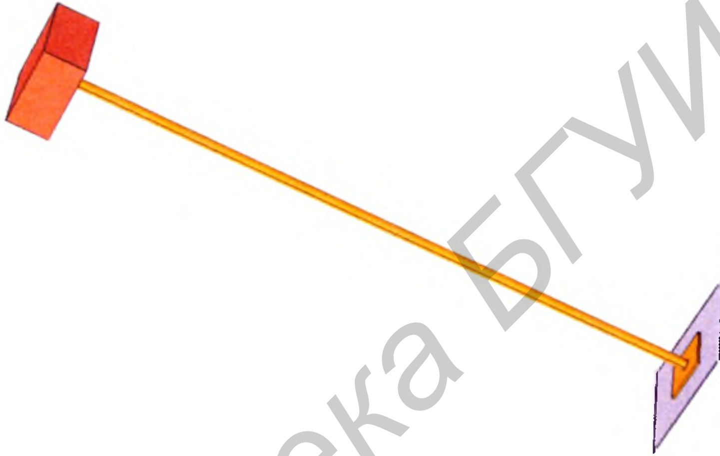

Figure C.5. Simplified three-dimensional model of the system of integrated circuits' current-carrying elements for the analysis of thermal unsteadiness distribution

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Table C.4. Values of temperature, electric field strength and electromagnetic losses power at the discharge voltage of 2 kV

Area	Test poing	Distance between points, μ*m*	Temperature, *K*	Electric field strength, *W/m*	Electromagnetic losses power, $W/m^3 \times 10^{16}$
External pin	1	25	293	100	0,1
	2	50	293	200	0,1
	3	75	294	250	0,3
	4	100	296	2500	0,2
	5	115	297	7600	0,5
Traverse	6	125	303	11300	0,5
	7	200	303	11300	0,5
	8	600	303	11300	0,5
	9	1000	303	11300	0,5
	10	1400	303	11300	0,5
Contact pad	11	1550	302	11300	0,5
	12	1580	301	6900	0,4
Metallized tracks	13	1600	296	3300	0,1
Semiconductor chip	14	1700	293	2500	0,1

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Table C.5. Values of temperature, electric field strength and electromagnetic losses power at the discharge voltage of 4 kV

Area	Test point	Distance between points, μm	Temperature, *K*	Electric field strength, *W/m*	Electromagnetic losses power, $W/m^3 \times 10^{16}$
External pin	1	25	293	100	0,1
	2	50	293	200	0,1
	3	75	294	1000	0,3
	4	100	304	2600	0,3
	5	115	310	19100	1,7
Traverse	6	125	327	21900	2,2
	7	200	327	21900	2,2
	8	600	327	21900	2,2
	9	1000	327	21900	2,2
	10	1400	327	21900	2,2
Contact pad	11	1550	327	21900	2,2
	12	1580	325	20100	1,8
Metallized tracks	13	1600	296	3300	0,3
Semiconductor chip	14	1700	293	5500	0,1

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Table C.6. Values of temperature, electric field strength and electromagnetic losses power at the discharge voltage of 6 kV

Area	Test point	Distance between points, p*m*	Temperature, *K*	Electric field strength, *W/m*	Electromagnetic losses power, $W/m^3 \times 10^{16}$
External pin	1	25	293	100	0,1
	2	50	293	600	0,1
	3	75	294	2300	0,3
	4	100	304	4600	0,3
	5	115	345	24900	3,7
Traverse	6	125	368	33 400	4,9
	7	200	368	33 400	4,9
	8	600	368	33 400	4,9
	9	1000	368	33 400	4,9
	10	1400	368	33 400	4,9
Contact pad	11	1550	360	33 400	4,9
	12	1580	325	30 100	4,1
Metallized tracks	13	1600	296	3300	0,3
Semiconductor chip	14	1700	293	8500	0,1

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Table C.7. Values of temperature, electric field strength and electromagnetic losses power at the discharge voltage of 8 kV

Area	Test point	Distance between points, μ*m*	Temperature, *K*	Electric field strength, *W/m*	Electromagnetic losses power, В/м³×10¹⁶
External pin	1	25	293	100	0,1
	2	50	293	1000	0,1
	3	75	294	3400	0,3
	4	100	304	5600	0,3
	5	115	395	36 800	3,7
Traverse	6	125	426	44 200	4,9
	7	200	426	44 200	4,9
	8	600	426	44 200	4,9
	9	1000	426	44 200	4,9
	10	1400	426	44 200	4,9
Contact pad	11	1550	426	44 200	4,9
	12	1580	426	41 600	4,1
Metallized tracks	13	1600	296	3300	0,3
Semiconductor chip	14	1700	293	11 500	0,1

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Table C.8. Values of temperature, electric field strength and electromagnetic losses power at the discharge voltage of 15 kV

Area	Test point	Distance between points, μm	Temperature, *K*	Electric field strength, *W/m*	Electromagnetic losses power, $W/m^3 \times 10^{16}$
External pin	1	25	293	100	0,1
	2	50	293	1000	0,1
	3	75	294	3400	0,3
	4	100	304	5600	0,3
	5	115	395	36 800	3,7
Traverse	6	125	426	44 200	4,9
	7	200	426	44 200	4,9
	8	600	426	44 200	4,9
	9	1000	426	44 200	4,9
	10	1400	426	44 200	4,9
Contact pad	11	1550	426	44 200	4,9
	12	1580	426	41 600	4,1
Metallized track	13	1600	296	3300	0,3
Semiconductor chip	14	1700	293	11 500	0,1

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APPENDIX D

The principles of the hash-codes formation of the data array recorded into the built-in flash memory of microcontrollers

D.1. The principles of the hash-codes formation by MD5 algorithm

The input of the algorithm receives the data flow, the hash of which should be founded, and then goes the process of preparing the flow for calculations (figure D.1) [152].

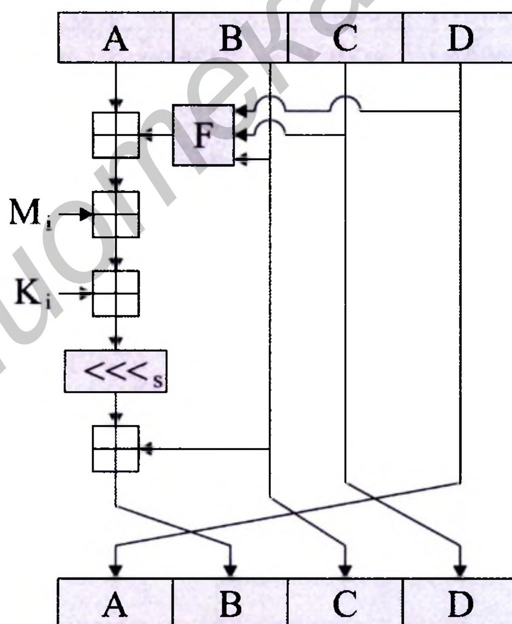

Figure D.1. Scheme of MD5 algorithm

The 5 steps of the algorithm are listed below:

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1. Alignment of the flow.

First, on-bit is appended to the end of the flow (byte 0x80), then the required number of off-bits is appended. Input data are aligned, so that their new size was comparable to 448 modulo 512 (L'=512×N+448).

7. Addition of the message length.

The 64-bit representation of the data length before the alignment is appended into the remaining 64 bits. First, 4 low bytes are recorded. If the length is more than $2^{64}-1$, then only the low bits are appended. Thereafter, the flow length becomes divisable by 512. Further calculations will be based on the representation of this data flow as the array of 512-bit words.

8. Buffer initialization

For the calculations 4 variables size of 32 bits are initialized and the initial values are set by hexadecimal numbers, starting with the low byte.

9. Calculation in the cycle

Element n from the array is entered to the data block. Values A, B, C and D, left after the operation on the previous blocks, are saved. Then summation is performed with the result of the previous cycle: After the end of the cycle the check is performed whether there are more blocks for calculations. If yes, then the array element number is changed and cycle starts from the beginning.

10. The result of calculations

The calculation result outputs byte by byte, starting with the low byte A and finishing with the high byte D, so MD5-hash is formed.

D.2. The principles of the hash-codes formation by SHA-1 algorithm

SHA-1 algorithm implements hash-function based on the idea of the compression function, inputs of which are the message block length of 512 bits and the output of the previous message block. The output is the value of all hash-blocks up to this point (figure D.2) [153].

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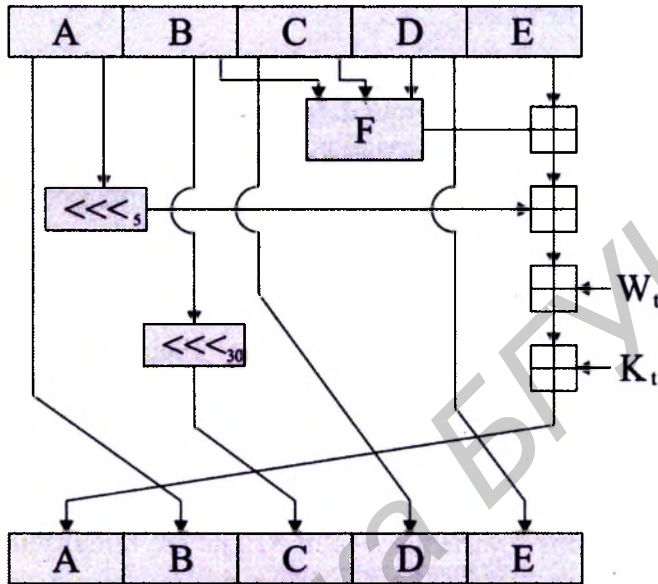

Figure D.2. Scheme of SHA-1 algorithm

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The initial message is divided into blocks of 512 bits each. The last block is appended up to the length of a multiple of 512 bits. First, 1 is added, then zeroes, so the block length becomes equal to (512–64 = 448) bytes. The length of the initial message in bits is recorded into the remaining 64 bits. The last block is always appended, even if the message already has the necessary length.

The final value is the combination of five 32-bit words in a 160-bit hash value.

APPENDIX E

Reference data for the calculation of the tested microcontrollers' operational failure rate

Table E.1. Die base failure rate λ_{BD}

Part type	λ_{BD}
Logic and custom	0,16
Gate array	0,24

Table E.2. Manufacturing process correction factor ϖ_{MFG}

Manufacturing process	ϖ_{MFG}
QML or QPL	0,55
Non QML or non QPL	2,0

Table E.3. Junction to case thermal resistance ϑ_{JC} for a device soldered into a printed circuit board

Package type (ceramic only)	Die area > 14400 mil^2 θ_{JC}, (°C/W)	Die area ≤ 14400 mil^2 θ_{JC}, (°C/W)
Dual-in-line	11	28
Flat package	10	22
Chip carrier	10	20
Pin grid array	10	20
Can	–	70

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Table E.4. Temperature factor for all microcircuits ϖ_T

	TTL, ASTTL, CML, HTTL, FTTL, DTL, ECL, ALSTTL	F, LTTL, STTL	BiCMOS, LSTTL	III, I^3L, ISL	Digital MOC, VHSIC CMOS	Linear (Bipolar & MOS)	Memories (Bipolar & MOS), MNOS	GaAs MMIC active devices, ϖ_{TA}	GaAS digital active devices, ϖ_{TA}
E_a (eV) → T_J (°C)	0,4	0,45	0,5	0,6	0,35	0,65	0,6	1,5	1,4
25	0,10	0,10	0,10	0,10	0,10	0,10	0,10	3,20E-09	1,00E-08
30	0,13	0,13	0,14	0,15	0,13	0,15	0,15	8,40E-09	2,50E-08
35	0,17	0,18	0,19	0,21	0,16	0,23	0,21	2,10E-08	5,90E-08
40	0,21	0,23	0,25	0,31	0,19	0,34	0,31	5,20E-08	1,40E-07
45	0,27	0,3	0,34	0,43	0,24	0,49	0,43	1,30E-07	3,10E-07
50	0,33	0,39	0,45	0,61	0,29	0,71	0,61	2,90E-07	6,80E-07
55	0,42	0,50	0,59	0,85	0,35	1,0	0,85	6,70E-07	1,50E-06
60	0,51	0,63	0,77	1,2	0,42	1,4	1,2	1,50E-06	3,10E-06
65	0,63	0,80	1,0	1,6	0,50	2,0	1,6	3,20E-06	6,40E-06
70	0,77	1,0	1,3	2,1	0,60	2,8	2,1	6,80E-06	1,30E-05
75	0,94	1,2	1,6	2,9	0,71	3,8	2,9	1,40E-06	2,50E-05
80	1,1	1,5	2,1	3,8	0,84	5,2	3,8	2,90E-06	4,90E-05
85	1,4	1,9	2,6	5,0	0,98	7,0	5,0	5,70E-06	9,40E-05
90	1,6	2,3	3,3	6,6	1,1	9,3	6,6	1,10E-04	1,70E-04
95	1,9	2,8	4,1	8,5	1,3	12	8,5	2,10E-04	3,20E-04
100	2,3	3,4	5,0	11	1,5	16	11	4,00E-04	5,80E-04
105	2,7	4,1	6,2	14	1,8	21	14	7,50E-04	1,00E-03
110	3,2	4,9	7,5	18	2,1	28	18	1,40E-03	1,80E-03

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Table E.4 continuation

	TTL, ASTTL, CML, HTTL, FTTL, DTL, ECL, ALSTTL	F, LTTL, STTL	BiCMOS, LSTTL	III, I^3L, ISL	Digital MOC, VHSIC CMOS	Linear (Bipolar & MOS)	Memories (Bipolar & MOS), MNOS	GaAs MMIC active devices, ϖ_{TA}	GaAS digital active devices, ϖ_{TA}
115	3,7	5,8	9,2	23	2,4	35	23	2,40E-03	3,10E-03
120	4,3	6,9	11	28	2,7	45	28	4,30E-03	5,30E-03
125	5	8,2	13	35	3,1	58	35	7,50E-03	9,00E-03
130	5,8	9,6	16	44	3,5	73	44	1,30E-02	1,50E-02
135	6,7	11	19	54	3,9	92	54	2,20E-02	2,40E-02
140	7,7	13	23	67	4,4	120	67	3,70E-02	3,90E-02
145	8,8	15	27	82	5,0	140	82	6,10E-02	5,30E-02
150	10	18	32	100	5,6	180	100	1,00E-01	1,00E-01
155	11	20	37	120	6,3	220	120	1,60E-01	1,60E-01
160	13	24	43	150	7,0	270	150	2,60E-01	2,40E-01
165	15	27	50	180	7,8	330	180	4,10E-01	3,70E-01
170	16	31	59	210	8,7	400	210	6,40E-01	5,70E-01
175	18	35	68	250	9,6	480	250	9,90E-01	8,50E-01

$$\pi_T = 0{,}1\exp\left(\frac{-E_a}{8{,}617\times10^{-5}}\left(\frac{1}{T_J+273}\cdot\frac{1}{296}\right)\right)$$

Silicon devices

$$\pi_T = 0{,}1\exp\left(\frac{-E_a}{8{,}617\times10^{-5}}\left(\frac{1}{T_J+273}\cdot\frac{1}{423}\right)\right)$$

GaAs devices

E_a – effective activation energy (eV) (shown above);

T_J – worse case junction temperature (silicon device) of average active device channel temperature (GaAs devices).

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End of the table E.4

Notes:	1. $T_J = T_C + P\theta_{JC}$ 2. T_C – case temperature (°C); 3. P – device power dissipation (W); θ_{JC} – junction to case thermal resistance (°C/W); θ_{JC} should be obtained from the device manufacturer, MIL–M-38510, or from the default values shown in table E.4. for the closest equivalent device. Use digital MOS column for HC, HCT, AC, ACT, C and FCT technologies Table entries should be considered valid only up to the rated temperature of the component under consideration.

Table E.5. Die complexity factor ϖ_{CD}

Feature size (microns)	Die Area (cm²)				
	A ≤ 0,4	0,4 < A ≤ 0,7	0,7 < A ≤ 1,0	1,0 < A ≤ 2,0	2,0 < A ≤ 3,0
0,80	8,0	14	19	38	58
1,00	5,2	8,9	13	25	37
1,25	3,5	5,8	8,2	16	24

$\pi_{CD} = \left(\frac{A}{0,21} \cdot \left(\frac{2}{X_S} \right)^2 \cdot 0,64 \right) + 0,36$ A – total scribed chip die area in cm² X_S – feature size (microns)

Die area conversion: cm² = mil² + 155 000

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Table E.6. Package base failure rate λ_{BP}

Number of pins	λ_{BP}
24	0,0026
28	0,0027
40	0,0029
44	0,0030
48	0,0030
52	0,0031
64	0,0033
84	0,0036
120	0,0043
124	0,0043
144	0,0047
220	0,0060
$\lambda_{BP} = 0,0022 + ((1,72 \times 10^{-5}) \cdot N$ *NP* – number of package pins	

Table E.7. Package type correction factor ϖ_{PT}

Package type	ϖ_{PT}	
	Hermetic	Nonhermetic
DIP	1,0	1,3
Pin grid array	2,2	2,9
Chip carrier (surface mount technolody)	4,7	6,1

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Table E.8. Environment factor ϖ_E

Environment	ϖ_E
G_B	0,50
G_F	2,0
G_M	4,0
N_S	4,0
N_U	6,0
A_{IC}	4,0
A_{IF}	5,0
A_{UC}	5,0
A_{UF}	8,0
A_{RW}	8,0
S_F	0,50
M_F	5,0
M_I	12
C_L	220

Table E.9. Electrical overstress failure rate λ_{EOS}

V_{TH} (ESD susceptibility (Volts))*	λ_{EOS}
0–1000	0,065
> 1000–2000	0,053
> 2000–4000	0,044
> 4000–16000	0,029
> 16000	0,0027

$$\lambda_{EOS} = \left(-\ln\left(1-0,00057\exp\left(-0,0002V_{TH}\right)\right)\right)/0,00876$$

V_{TH} – ESD susceptibility (Volts)

* Voltage ranges which will cause the part to fail. If unknown, use 0–1000 volts.

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Table E.10. Quality factors ϖ_Q

Description	ϖ_Q
Class S categories: 1. Produced in full accordance with MIL–M-38510, Class S requirements. 2. Produced in full accordance with MIL–I-38535 and Appendix B thereto (Class U). 3. Hybrids: (produced to Class S requirements (quality level K) of MIL-H-38534.	0,25
Class B categories: 1. Produced in full accordance with MIL–M-38510, Class B requirements. 2. Produced in full accordance with MIL–I-38535, Class Q. 3. Hybrids: produced to Class B requirements (quality level H) of MIL-H-38534.	1,0
Class B-1 category: Fully compliant with all requirements of paragraph 1.2.1 of MIL-STD-883 and produced to a MIL drawing. DESC drawing or other government approved documentation. (Does not include hybrids).	2,0

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Научное издание

Пискун Геннадий Адамович
Алексеев Виктор Федорович
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**ВЛИЯНИЕ ЭСР
НА МИКРОКОНТРОЛЛЕРЫ**

Ответственный за выпуск *Е. С. Патей*
Компьютерная верстка *Д. С. Гавинович*

Подписано в печать 09.01.2018. Формат 70x100$^{1}/_{16}$.
Бумага офсетная. Печать цифровая. Усл. печ. л. 13,60.
Уч.-изд. л. 12,80. Тираж 120 экз. Заказ 7258.

Издатель и полиграфическое исполнение:
частное производственно-торговое
унитарное предприятие «Колорград».
Свидетельство о государственной регистрации издателя,
изготовителя, распространителя печатных изданий
№ 1/471 от 28.07.2015.

Пер. Велосипедный, 5-904, 220033, г. Минск,
www.сегмент.бел

Библиотека БГУИР

Scientific publication

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THE IMPACT OF ESD ON MICROCONTROLLERS

Publisher and printing perfomance
private production and trade
unitary enterprise «Kolorgrad».
Certificate of state registration of the pulisher,
manufacturer, distributor of publications
№ 1/471 from 23.12.2015.

5-904, Velosipedny Lane, Minsk, 220033,
www.сегмент.бел

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