DEEP SUBMICRON RADIATION HARDENED STATIC RANDOM-ACCESS MEMORY IP

A. Kostrov
Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus

I. INTRODUCTION

Modern System-on-a-Chip (SoC) is impossible to develop without built-in memory blocks. The availability of embedded memory enables SoC to perform fast, complex operations with large data arrays. Therefore the percentage of chip area occupied by various memories is constantly growing. Design of ICs which include large-scale memory blocks requires special software – IP Memory Block Compiler that would permit netlist and die topology to be created. Memory compilers allow quickly and automatically generate specifically sized memory blocks to be used in the design of ASICs.

Static Random-Access Memory (SRAM) is often embedded in microprocessor or microcontroller systems as their main memory component. SRAM permits quickly develop a highly reliable SoC required for spacecraft subsystems or instruments that are often used in extreme temperature and radiation environments, such as those in outer space, on the Moon and Mars. The reliability of electronics in the spacecraft becomes one of the most important concerns. Exposure to the high-energy subatomic particles and electromagnetic radiation may cause transient effects in memories such as glitches and soft errors, or permanent damage to the chip like lattice displacement, latch-up, or SEUs (single event upsets). Very-deep-submicron technologies with aggressive device and voltage supply downsizing have significantly reduced the critical charge required for bit storage in memory cells. This means low energy particles can flip the state in memory cells, therefore making memories sensitive to atmospheric neutrons as well as to alpha particles created from materials within the chip. In addition, the increased number and density of cells leads to increased probability of SEU occurrence.

To achieve acceptable SRAM memory radiation hardness, it may be necessary to employ one or more radiation impact mitigation techniques, such as radiation hardening by layout and circuit design, circuit/system redundancy, and/or data error correction codes. Under low radiation operating conditions or when the ASICs are shielded from radiation impact, radiation hardening means implemented into ASICs lead to sub-optimum performance. For example, radhard SRAM would be consuming much higher power – a precious resource in space missions. Therefore, space missions need a special memory compiler to be used. The compiler would permit designing ASICs targeted to tolerate required radiation levels and to be able to balance the radiation hardness, speed of operation and power consumption.

II. GENERAL INFORMATION

Pacific Microchip Corp. proposes to develop a novel configurable memory compiler for radiation hardened single port SRAM IP. The compiler will provide the choice between three types of memory cells that are based on 6-transistor (6T) improved architecture. The three memory cell designs will be aiming at different levels of immunity to radiation while consuming different levels of power. The novel compiler will implement such radiation hardening techniques and methods as:

- Radiation Hardening-By-Design (RHBD),
- Radiation Hardening-By-Layout (RHBL),
- Radiation Hardening-By-System (RHBS).

The radiation hardening means will include:

- N-channel Edge-Less Transistors (ELT) to mitigate Total Ionization Dose (TID) and Single Event Latchup (SEL);
- Miller capacitor connected between the two latches of the SRAM cell for mitigating Single Event Upset (SEU);

- PNPN parasitic thyristor triggering threshold increasing by adding guard rings for minimizing SEL;
- Bit interleaving for Multi-Bit Upset (MBU) mitigation;
- Single error correcting/double error detecting (SEC-DED) codes for SEU hardening;
- Triple-Modular Redundancy (TMR) with majority voters to reduce Single Event Transients (SET).

The proposed compiler features include:

1. The size of compiled memory SRAM: 8x2 bits (minimum), 32768x72 bits (2 Mb) (maximum)
2. Possible word width: from 4 to 72 bits with a step increment of 1 bit;
3. Word depth is from 8 to 32768 bits, depending on the width of the multiplexer.

Architectural flexibility of the compiled SRAMs will be achieved by using multiplexing to support a wide range of options in the aspect ratio of IP modules. Three levels of multiplexing will be supported: mux8, mux16, mux32. SRAM will have four control signals: 1) a user-defined non-inverting or inverting clock CE/CEB; 2) an output enabler (OEB); 3) a chip select (CSB); and 4) a read/write enable (WEB). Input and output data (I [n]) and (O [n]) will have separate ports. The output buffer circuit will be capable of operating in two user-defined modes: 1) a 3-states output and 2) a stable zero (hard “0”) output. OEB control will be used to switch between output data enable mode and one of the user defined modes.

For successful using of memory modules as parts of SOC, designer needs to have behavioral description including timings and power models in Synopsys format for further timing and power analysis. For this reason compiler has to provide accurate and fast algorithm for calculation of these parameters. A mathematical model will be developed to describe the dependence of delay and power consumption on the combination of input factors (number of words, bits, output load and the input signal slope). The regression model will be used to determine the changes in the IP module parameters such as delay and power consumption and the aggregate change in the input factors (words, bits, load, input slope).

The Phase I effort will focus on cell, critical peripheral circuit and layout design as well as on the radiation hardened SRAM architecture. As a result of this Phase I effort we will provide the proof of the feasibility of implementing the proposed novel memory IP compiler. During Phase II, we will develop the flexible and configurable compiler, create layout and circuit databases for compiler, fabricate and test the proposed memories designed to meet the stringent radiation hardness and optimized power consumption requirements of space missions. We anticipate our proposed memory will be implemented based on the currently available IBM 45nm SOI CMOS or 65/90nm bulk CMOS technology. Phase II will result in the SRAM IP compiler, with memory prototypes ready for commercialization in Phase III.

Potential space applications for SRAM include microprocessor or microcontroller systems required in navigation, communication, command and control for launch vehicles, payloads, satellites, and any other space flight system requiring survivability in natural space radiation environments. Other systems used in space missions that require the storage of significant quantities of information include battery powered wearable electronics, portable monitors and devices. These systems would benefit from the proposed SRAM complied for minimum power consumption while trading the radiation hardness.

CONCLUSIONS

The proposed memory compiler will be used to design integrated memory arrays based on specifications defined through developed graphical user interface. The methodology for application of the memory compiler will also be prepared. As a result, we will provide a data file required for a specified type of the SRAM memory arrays.

The proposed novel memory compiler of radiation hardened SRAM IP offers a flexible solution for SoC and ASICs to meet the stringent radiation, performance, size and weight requirements of space applications.