DEVICE AND TECHNOLOGY SIMULATION OF IGBT ON SOI STRUCTURE

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Abstract – Static and dynamics characteristics of the power IGBT device at "Silicon-On-Insulate" structure were simulated. Analysis of the characteristics of such structure in comparison with the IGBT at the bulk silicon are presented. Advantages of IGBT device at SOI are revealed.

I. INTRODUCTION

At present two base types of power electronics contemporary devices are dominant: field transistors (Metal Oxide Silicon Field Effect Transistor, MOSFET) and bipolar transistors with the isolated gate (Isolated Gate Bipolar Transistor, IGBT), as well as various integrated structures on their basis. The numerous requirements to the power electronic systems (low losses during switches, small voltage drop in the activated state, high resistance in the off-state, high efficiency, etc.) stimulate researches for the new design structures, fabrication technologies, materials of the structural elements of such devices and layouts. IGBT due to its exceptional functional features, combining the positive properties of power field and bipolar transistors, is a widely applied power device and finds a wide application in the devices of the electric thrust and AC motors, induction heating systems, radiological systems, power back-up sources, switching elements. Perfecting of the IGBT structures is oriented at enhancing the efficiency, limit commutating currents and voltages.

II. TECHNOLOGY «SILICON–ON-INSULATOR»

The technology «Silicon–On-Insulator» (SOI) was elaborated specifically to obtain the devices of the high temperature electronics and applications, requiring resistance to influence of the hard radioactive irradiation. In the structures "silicon-on-insulator" the working layer of silicon is separated from the substrate by means of the dielectric isolating layer of silicon oxide.

The SOI technology resolves a number of problems, emerging in the structures on the bulk silicon at high temperatures. The essence of technology is essentially in the complementary oxygen implantation into the silicon substrate with formation of the dielectric layer of silicon oxide inside the semiconductor.

The SOI structures are distinguished for their high radiation resistance and enhanced reliability at high temperatures. The short channel effects in the SOI devices can be suppressed by a mere reduction of the silicon layer thickness. The tilt of the above threshold characteristic of the SOI transistors is derived practically ideal. The high quality transistors are attained on the silicon films 8 nm thick.

For the SOI structures three methods of isolation are used: local silicon oxidation (LOCOS), isolation by means of shallow trenches (STI) and meza-isolation. The LOCOS – isolation is hard to use with the design rules of less than 0,25 μm due to the «bird's beak», which limits the potentialities of obtaining the small area isolating regions. The STI–isolation is a relatively expensive process.

III. SIMULATED STRUCTURE

Earlier there had been conducted researches devoted to investigation of the static and dynamic IGBT features dependence on the technology parameters at manufacturing of IGBT structure in bulk silicon. Thickness of the epitaxial layer of such structure was selected to be equal to 141 μm, and thickness of the p^+–collector layer – 17 μm, as in work [1].

From the entire variety of the possible IGBT structures on SOI, described in the literature [2-6] the IGBT structure was selected, represented in Figure 1, a.

The transistor base is essentially the silicon film, located on the isolation material. IGBT may possess any polarity: a bipolar transistor of the pnp-type with n-MOS transistor or a bipolar transistor

of the npn-type with a p-MOS transistor. A greater current density in the IGBT structures is attained by means of the formed n-well of the source, increasing the base current of the bipolar transistor in IGBT. The gates can control one or two channels of the MOS transistors. The vertical sizes of the n-type of the drift area are augmented to enhance the current density without growth of the voltage drop value in the n-drift region.

Simulation of the technology flow of the IGBT on SOI structure manufacturing was performed using the SILVACO package [7] in compliance with the last trends in the IGBT on SOI technology [8-9].

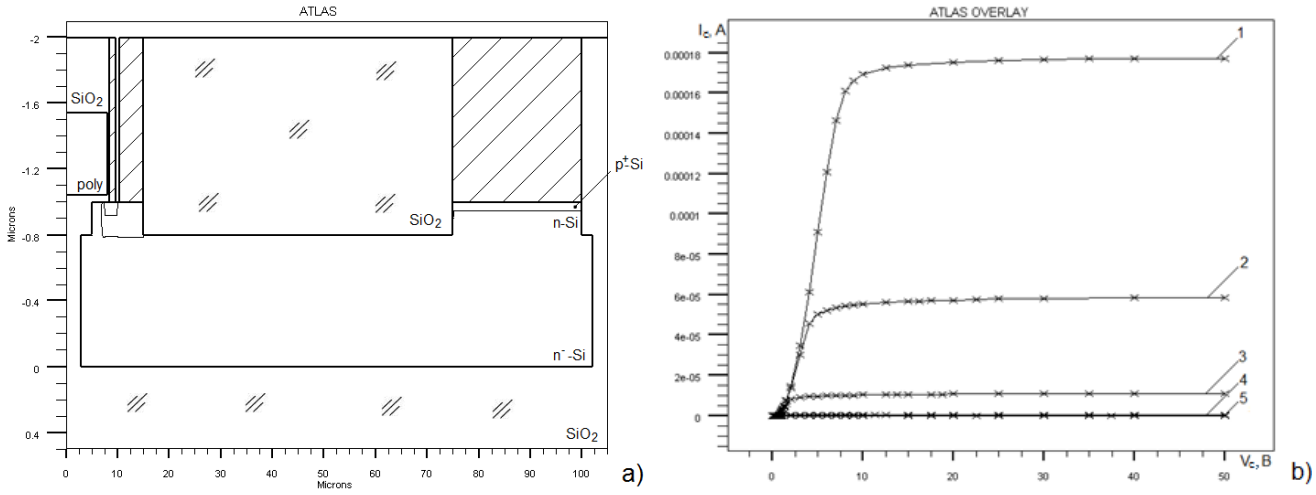

Figure 1 – Structure of the IGBT on the SOI (a) and Dependences of collector current I_c on collector voltage V_c for the structures with various h_{ox}: 1 – h_{ox}=30 nm; 2 – h_{ox}=40 nm; 3 – h_{ox}=50 nm; 4 – h_{ox}=60 nm; 5 – h_{ox}=70 nm

IV. RESULTS

The I-V features were obtained with the various thickness values of the gate h_{ox} (Figure 1, b). The thickness was varied within the limits from 30 to 70 nm.

Thickness of the gate oxide exerts a significant influence on the electric parameters of IGBT on SOI. With reduction of the oxide thickness from 40 nm down to 30 nm the bipolar transistor base current is increased and, thus, the saturation current value of the collector is increased (from ≈ 55 μA to ≈ 175 μA). Meanwhile, the switch-on time for the both IGBT structures stays equal to 25 ns, and the switch-off time rises from 55 ns for h_{ox}=40 nm to the value of 75 ns h_{ox}=30 nm.

The calculated values of the switch-on and switch -off durations are by an order smaller (25 ns and 75 ns for IGBT on SOI structure and 350 ns and 870 ns for the IGBT on the bulk silicon respectively), Withal the current value of the collector (30 μA) is greater by an order than for the vertical IGBT structure on the basis of the bulk silicon (4 μA).

V. CONCLUSION

Results of the technology design for the manufacturing of the bipolar transistor with the isolated gate (IGBT) at the “Silicon On Insulator” and at the bulk silicon structures [10] are presented. Comparisons of I-V features and dynamic characteristics (switch-on and switch-off durations) for both device constructions were carried out. on whose basis optimization was carried out of the design-process parameters on an example of such a parameter, as thickness of the gate oxide. It was shown, that thickness of the gate oxide exerts a substantial influence on the IGBT electric parameters. With reduction of the oxide thickness h_{ox} from 40 nm down to 30 nm the base current of the bipolar transistor increases and, thus, the saturation current value of the collector rises (from ≈ 55 μA to ≈ 175 μA). Meanwhile, the switch-on time for the both IGBT structures stays equal to 25 ns, and the switch-off time is increased from from 55 ns for h_{ox}=40 nm to the value of 75 ns for h_{ox}=30 nm.

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