

CONCEPT OF NEW COMPACT MODEL OF DEEP-SUBMICRON MOSFET

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Abstract – Concept of new compact model for the simulation of deep submicron (DSM), nanometer-scale MOSFET transistor characteristics is presented. The proposed model is based on the use of traditional “compact” submicron MOSFET device model. Parameters of this model are verified by means of fitting procedure to results obtained by use exact physical models taking into account quantum effects accompanying charge carriers transfer in DSM MOSFET.

I. INTRODUCTION

In microelectronics today, difficulties of integrated circuit and technology design are rising; integrated circuit complexity is increasing; die areas are also getting larger in order to incorporate the increasing of functionality... Integrated circuit design in micro- and nanoelectronics is based on the solution of complex problem of charge carriers transport simulation in the device structure. The problem is becoming even more acute in design of deep submicron (DSM), below 0.13 μm , where quantum-mechanical effects and accompanying leakage currents have to be taking into account.

Obviously, how consistently the physical effects have described in a certain model will determine how adequate the object/process simulation results will be compared to their real behavior. But the more exact the physical model is, the more strict mathematical methods (mostly numerical) are used for its implementation, and the more sophisticated and bulky computer facilities will be required for calculation.

There is a well-proved approach in microelectronics to reduce the necessary computing resources without the need to sacrifice the essential simulation accuracy, especially SPICE-like package. The essence of this approach is in replacing exact physical models by so-called compact models [1]. The basic feature of the compact models, as usually, is the use of polynomials instead of integral-differential equations, describing the processes under study. The coefficients of the polynomial series are “extracted” using the response-surface methodology, RSM from a limited amount of computer calculations based on the exact physical models or from full-scale experiments, employing specific “design of experiments” (DOE methodology [2]).

In this work authors propose an approach for calculation the I-V characteristics of deep submicron, nanometer MOS transistors, based on use of generalized compact model. The proposed new compact model was proved by using the Silvaco package [3], intended for technology and device design of microelectronic products.

II. COMPACT MODEL FOR DEEP SUBMICRON MOS-FET. METHODOLOGY

The problem of parameter extraction of device models used in program complex Silvaco, can be reduced to the task of the conditional optimization. That procedure is in seeking of the minimum extent of discrepancy between the result calculated with exact physical model and compact model approach, where the model parameters appear as the appropriate factors.

The physical models of semiconductor devices are described by system of equations (1), which link the electrostatic potential ψ with the carriers density ρ

$$\left. \begin{aligned} \operatorname{div}(\epsilon \nabla \psi) &= -\rho, \\ \vec{E} &= \nabla \psi, \\ \frac{\partial n}{\partial t} &= \frac{1}{q} \operatorname{div}(\vec{J}_n) + G_n - R_n, \\ \frac{\partial p}{\partial t} &= \frac{1}{q} \operatorname{div}(\vec{J}_p) + G_p - R_p, \end{aligned} \right\} \quad (1)$$

To determine carrier density, the charge transport equations are used. The simplest charge transfer model for the calculation of I-V device characteristics is the drift-diffusion (DD) model, described by drift-diffusion equations (2):

$$\left. \begin{aligned} \bar{J}_n &= qn\mu_n\bar{E}_n + qD_n\nabla n \\ \bar{J}_p &= qp\mu_p\bar{E}_p - qD_p\nabla p \end{aligned} \right\} \quad (2)$$

Until recently, the drift-diffusion model was adequate for nearly all devices that were technologically feasible. The drift-diffusion approximation, however, becomes less accurate for smaller feature sizes. More advanced models taking into account quantum effects in deep submicron devices are needed. Such models were developed in the frame of Silvaco package. They are Energy Balance and Hydrodynamic models. Silvaco package supplies both drift-diffusion and advanced transport models. Beside Silvaco models more advanced models also support, which are accounting for quantum effects, to supply simulation of nanoscale devices, for example, Monte-Carlo methodology.

Differences between results of simulation in Silvaco DD model both Monte-Carlo calculations and experiment in sub-micron (0.25 μm) and deep sub-micron (0.1 μm) MOS transistor are shown in Fig. 1 [4].

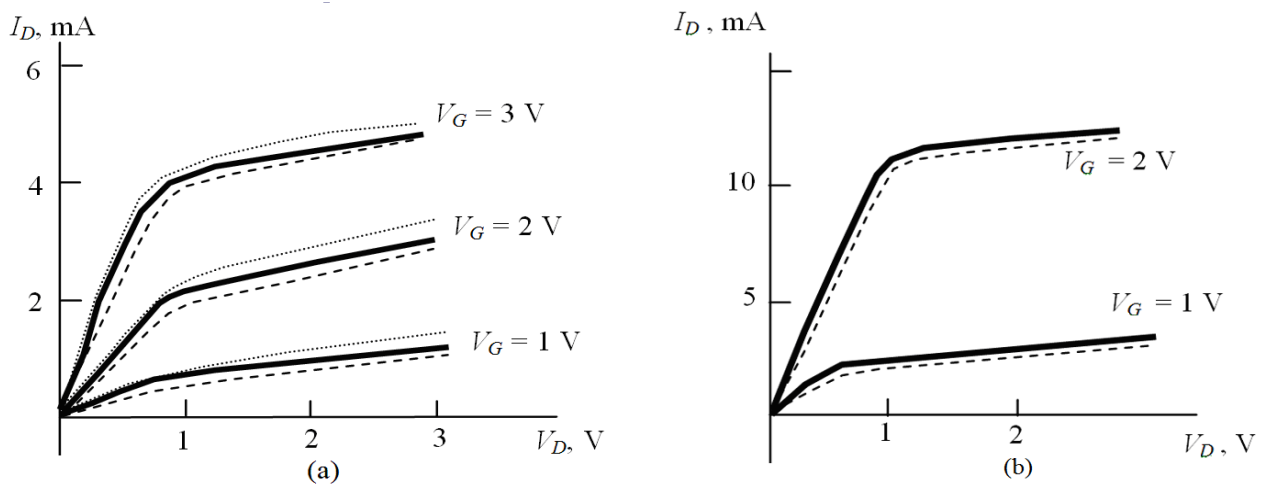


Figure 1 – The dependencies drain current - drain voltage (I_D vs V_D) of MOS transistor (a) 250 nm and (b) 100 nm channel length: solid – experiment; dashed – Monte Carlo (MC) simulation; dotted – Silvaco simulation result

In DD models the carrier mobility is the main factor influenced on the transport process of the charge carriers in the MOSFET structure. We proved in the frame of the carrier mobility Darwish model [5] that only some parameters of the carrier mobility model affect on the I-V characteristics of MOS structures stronger in comparison with others. Such parameters (so called “significant” parameters) are calculated with use screening experiments by means of design of experiment methodology [6]. Our results, presented in Fig. 2, show a wide change of I-V characteristics MOSFET (~ 3.5 times) while parameters of mobility Darwish model are only varied 20% from their default values. That fact illustrates the possibility of propose compact model to describe I-V features of deep submicron MOS transistor.

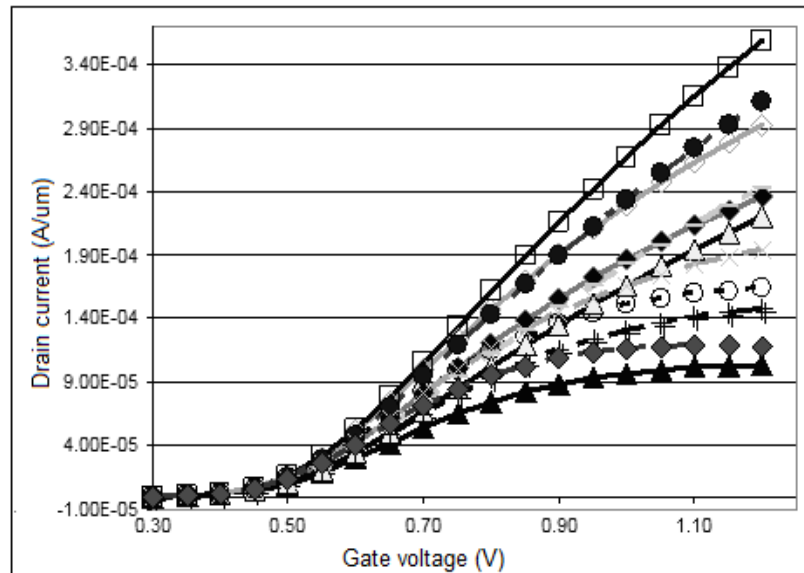


Figure 2 – I-V characteristics of 100nm MOSFET with various combinations of parameters from Darwish mobility model

III. CONCLUSION

Concept of new compact model for simulation of deep submicron MOS I-V characteristics is described. The methodology is based on traditional ideology of compact models. The new model could apply into all device simulation frameworks which include traditional drift-diffusion model of charge carriers for DSM-device simulation.

ACKNOWLEDGMENT

The work has been supported by the Grant in the frame of Belarusian Government Research Program “Electronics and Photonics” – task 1.1.03.

REFERENCES

- [1] Denisenko V., *Compact MOS transistor models for SPICE in micro- and nanoelectronics* / Moscow, Fizmatlit, 2010. 407 p.
- [2] Kouleshoff A., Malyshev V., Nelayev V., and Stempitsky V. “Statistical design and optimization of integrated circuits manufacturing”, *Russian J. Microelectronics*, 2003. vol. 32. No. 31. pp. 47–61.
- [3] <http://www.Silvaco.com>
- [4] Belous A., Nelayev V., Shvedov S., Stempitsky V., Tuan Trung Tran, Turtsevich A., “Compact DSM MOSFET model and its parameters extraction,” Proc. of the Int. Symposium East-West Design Testing (EWDTS’2011), Ukraine, 2011, pp. 230–232.
- [5] Darwish M. “An improved electron and hole mobility model for general purpose device simulation,” *IEEE Trans. on Electron. Dev.* 1997, vol. 44, № 09, pp.1529–1538.
- [6] Stempitsky V. Verification of significant parameters in the deep-submicron MOS-FET simulation / Stempitsky V., Tran Tuan Trung, Borovik A. // Proc. of The XII Int. Conf. The Experience of Designing and Application of CAD Systems in Microelectronics (CADSM’2013), Ukraine.– 2013.– P. 351–354.