Physic-topological (electrical) model of a junction field effect transistor, taking into account the degradation of operational characteristics under the influence of penetrating radiation

Ivan Lovshenko[1,*], *Veranika* Khanko[2], and *Viktor* Stempitsky[3]

[1]Micro- and nanoel. dept., Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus, lovshenko@bsuir.by
[2]Research Laboratory 4.4, Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus, hanko@bsuir.by
[3]R&D Department, Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus, vstem@bsuir.by

Abstract. The results of applying the compact model of junction field effect transistors developed and integrated into the Cadence software product for control to evaluate the hardness of a two-stage differential amplifier circuit under the combined or separate exposure to fluences of electrons, protons and neutrons are presented.

1 Introduction

The main factors of space environment that can cause damage to the electronics of spacecraft are the following [1]: ionizing radiation; cosmic plasma; thermal radiation of the Sun, planets and space environment; weightless state; etc. Ionizing radiation consists of a stream of primary charged nuclear particles - electrons, protons and heavy charged particles, as well as secondary nuclear particles - products of nuclear transformations associated with primary particles. The main effects of ionizing radiation on the electronics are associated with ionization and nuclear energy losses of primary and secondary particles in active and passive areas of semiconductor devices and integrated circuits (ICs).
The methods for assessing and predicting the hardness of ICs are based on studies of mechanisms the influence of penetrating radiation, which are manifested in radiation effects in semiconductors and structures with p-n-junctions: discomposition effect, nuclear transformations, ionization effects [2]. Discomposition effect lead to the formation of radiation defects in the crystal. A radiation defect can occur if the energy of bombarding particle is sufficient to displace the atom from the site of the crystal lattice to the interstitial site. On the operational characteristics device structures of n- and p-channel junction field effect transistors (JFET) are most affected by discomposition effects [3].

* Corresponding author: lovshenko@bsuir.by

2 Analysis of compact models JFET

Compact models, or models in the form of equivalent circuits (EC), today make up most of the models presented in CAD. [4]. When developing a compact model, one has to overcome the contradiction between its accuracy and speed. The term "structural models" has also gained some distribution, he emphasizes that the model in some way reflects the internal structure and physical features of the original object, in contrast to the so-called "structureless" or behavioral models. [5]. Compact models are divided into physical and formal. Some researchers single out tabular models into a separate class.

Compact physical models are created as a result of analysis physical processes, flowing in a semiconductor device. The fundamental principles of device's operation are used as the basis for the phenomenological equations that describe behavior of transistor relative to its electrodes using qualitative and quantitative physical macroscopic parameters. The following values can be used as parameters: thickness of the active semiconductor layer, gate length, doping of the active layer, electron mobility, gate oxide layer thickness, etc. Classical examples of this approach are the JFET field effect transistor model for silicon transistors, the most famous of which is the Shichman – Hodges model [6].

In modern software systems for device and circuit simulation, several JFET models are used, which are a continuation of the Shichman – Hodges model. Consider the models used in two widely used SPICE platforms: Silvaco SmartSpice [7] and Cadence Specter [8].

In particular, SmartSpice [9, 10] provides two JFET models: the basic SPICE model with improvements at the University of Sydney (Level 1) and the modified SPICE model that takes into account LAMBDA modulation (Level 2). Although the SmartSPICE Level 1 model is very similar to the traditional model, it has several advanced features: it takes into account temperature compensation and allows the calculation and scaling of geometry.

Model describes the characteristics of a JFET using two ideal diodes, two non-linear capacitors, three linear resistors and a current source. The ohmic resistance of the drain, gate, and source regions is represented by linear resistors RD, RG, and RS. In these models, there is the possibility of scaling them, choosing the equation of diffusion capacity, or changing the parameters of the model. The model includes a number of equivalent models of transistor operation modes: constant, variable, transitional and noise.

The model used in the Cadence Specter [11] implements many options and features. However, most of these additions do not apply to the physics that underpins modern JFETs. Recently, modern JFET models have appeared which are not standardized, but can significantly expand the capabilities of standard models. So, for example, SIMPLIS Technologies [12] developed for the SIMulation circuit simulator of proprietary JFET models that have several levels (levels 0, 1, 2, and 3) to adjust the speed and accuracy of the simulation. A four-pole compact model of the JFET [13, 14], which describes the steady-state characteristics with a single equation for all voltage conditions on the electrodes and includes the equations of capacitances and leaks is presented in the works. The model was implemented in Verilog-A and modeled in the Cadence system for comparison with experimental data measured in Texas Instruments.

The paper presents [15] various methods and principles of modeling and measuring the gate capacitance of JFET; the importance of matching equivalent models for different transistor operation modes is considered; methods of correcting well-known models to improve accuracy in calculations are proposed. The same authors developed a four-pole behavioral model written in the Verilog-A hardware description language [16]. This model has good convergence parameters, the simulation speed is comparable to conventional compact models and takes into account three-dimensional parasite effects.

In addition to traditional silicon, much attention is paid to the development of models JFET based on promising semiconductor materials such as silicon carbide SiC and graphene.

Case Western Reserve University [17] has developed the SPICE and Verilog-A of SiC model JFET, which use refined models of charge carrier mobility and capacity and optimized parameter sets.

The article presents [18] the simulation results of graphene-based JFETs, showing a five-fold speed advantage over silicon-based structures formed using 32 nm technology. The calculations are based on the JFET model, which is valid for devices based either on a monolayer of graphene or on two-layer graphene, the effectiveness of which allows us to develop and analyze logic circuits consisting of many graphene devices. Modeling shows that this model is closely related to experimental data.

Unfortunately, the use of SPICE-like IC simulation programs is limited, as a rule, by standard circuit models that do not provide an effective account of radiation effects.

3 Structure

JFET belong to the category of normally open field-effect transistors, in which the conducting channel and, consequently, the current in the channel, close to the maximum, exist at zero gate voltage ($V_G = 0$ V). These JFET are called depleted-type devices, since when the voltage is applied to the gate, the channel is depleted by electrical current carriers and the current in the channel decreases. Device structure of the p-JFET is shown in Fig. 1. Substrate of the hole type conductivity, doped boron with concentration of $1{,}35 \cdot 10^{15}$ cm-3, crystallographic orientation (111).

In the modelling of the operation-routing sequence for the formation of the device structure p-channel JFET, 14 stages are conventionally allocated: setting the parameters of the substrate and selecting computation grid, sequential formation of regions of the n^+-buried layer, p^+-buried layer, epitaxial layer, oxide isolation process, p-channel areas, n-collector, p^+-collector, p-base, opening of the areas under the contacts (together with oxidation of the substrate surface), formation of regions n^+-gate, p^+-emitter, n^+-emitter, 1st level of metal interconnections. To form the structure, 11 operations of photolithography are necessary.

The conditions for the application of the JFET imply the need to study the effect of penetrating radiations over a wide temperature range (from 383 K to 163 K). To obtain adequate results, it is necessary to correct the coefficients of the Klassen mobility model used in the simulation. The results of simulation electrical characteristics showed an acceptable agreement with the experimental data in the temperature range from 383 K to 223 K. Pinch-off voltage at 303 K is 1,31 V (measured at 1,29 V), the drain current is 3.9 mA (3.4 mA), for temperatures 383 K and 223 K the magnitude of these characteristics is 1.49 V (1.43 V) and 2.85 mA (2.7 mA), 1.17 V (1.15 V) and 4.58 mA (2.68 mA), respectively.

As shown in [3], there is a combination of fluence values and particle energy at which the effect is equal. It is assumed that the fluence of electrons F_E with an energy $E_E = 4$ MeV will cause in the IC the same displacements of atom as fluence of neutrons $F_N = 0{,}302\ F_E$ with an energy $E_N = 1{,}5$ MeV or fluence $F_P = 1{,}1 \cdot 10^{-4}\ F_E$ with an energy $E_P = 2{,}0$ MeV. Results of the effects fluence of electrons $F_E = 6 \cdot 10^{14}$ cm^{-2} with an energy $E_E = 4$ MeV and the corresponding fluences of neutrons and protons at a temperature 303 K and gate voltage $V_G = 0$ V is showned on the Fig. 2.

As can be seen from the figure, the effect of penetrating radiation with the parameters described above introduces almost identical degradation changes in the device structure. Thus, the drain current I_D of the p-channel JFET under the influence of the fluence of electrons $F_E = 6 \cdot 10^{14}$ cm^{-2} with an energy of $E_E = 4$ MeV decreases by 5.68 % with respect to the drain current of the JFET without exposure of penetrating radiation ($I_D = 3{,}70$ mA to $I_D = 3.49$ mA). For a fluence of neutrons $F_N = 2 \cdot 10^{14}$ cm^{-2} with an energy $E_N = 1{,}5$ MeV,

the change in the drain current is 4,59 % (drain current value I_D = 3,53 mA). For a fluence of protons $F_P = 6{,}6 \cdot 10^{10}$ cm^{-2} with an energy E_P = 2 MeV, the change in the drain current is 4,87 % (drain current value I_D = 3,52 mA).

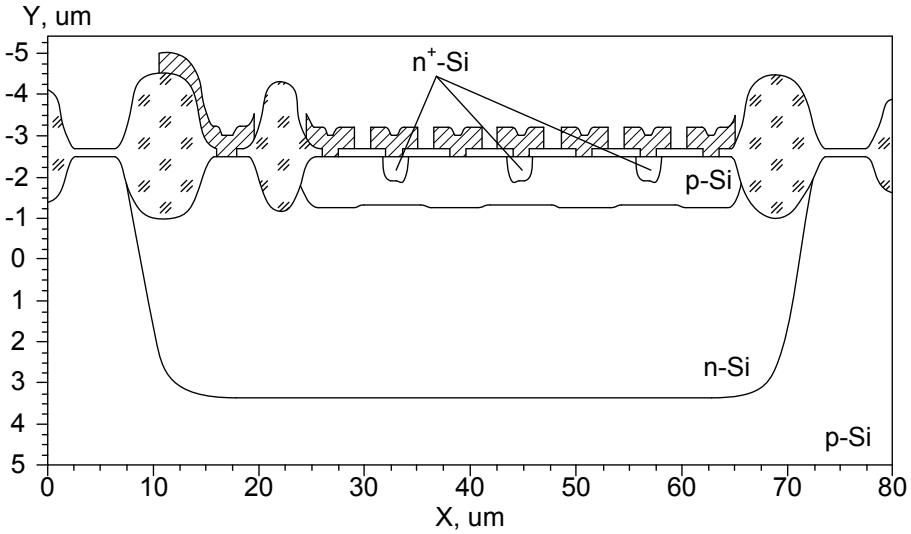

Fig. 1. Device structure of p-channel JFET.

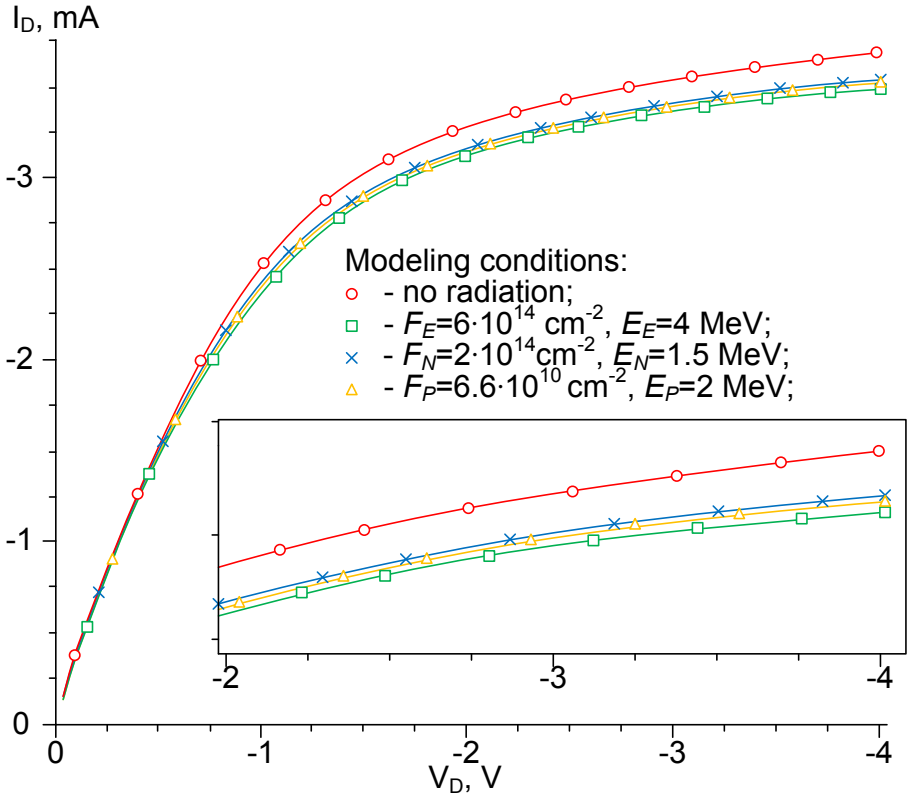

Fig. 2. Dependence of the drain current on the drain voltage VD when exposed to various types of penetrating radiations at a temperature 303 K.

4 Compact model

The developed model is an implementation in the language of Verilog-a hardware description from the original model of Shichman-Hodges field-effect transistor [6] with an additional set for determining the correction coefficients of model parameters most affected by the penetrating radiation. Such a set is implemented for three types of particles (protons, neutrons and electrons), as well as for the evaluation of their joint effect, expressed as a superposition of the introduced degradation effects. The set includes parameters for taking into account the effect of fluences of the particles ELECTRON, PROTON, NEUTRON (can take values 0 or 1 and are used to select the type of acting particles); parameters FE (can take value from 0 to 6e16) and EE (from 3 to 5), FP (from 0 to 6.6e11) and EP (from 1 to 3), FN (from 0 to 2e15) and EN (from 1 to 2) set the fluence (cm^{-2}) and energy (MeV) of electrons, protons and neutrons, respectively. In addition to the listed parameters, the developed model uses groups of variables, used in the calculation of model parameters when exposed to particle fluences:

– superposition of the influence of penetrating radiation on model parameters: rVTO, rLDEL, rWDEL, rRD, rBETA, rLAMBDA;

– coefficient of parameter change depending on the fluence of electrons, protons and neutrons: k1eVTO, k1eLDEL, k1eWDEL, k1eRD, k1eBETA, k1eLAMBDA, k1pVTO, k1pLDEL, k1pWDEL, k1pRD, k1pBETA, k1pLAMBDA, k1nVTO, k1nLDEL, k1nWDEL, k1nRD, k1nBETA, k1nLAMBDA;

– coefficient of parameter change depending on the energy of electrons, protons and neutrons: k2eVTO, k2eLDEL, k2eWDEL, k2eRD, k2eBETA, k2eLAMBDA, k2pVTO, k2pLDEL, k2pWDEL, k2pRD, k2pBETA, k2pLAMBDA, k2nVTO, k2nLDEL, k2nWDEL, k2nRD, k2nBETA, k2nLAMBDA.

The coefficients of the change in the parameters are calculated from the approximation dependences obtained from the analysis of the results of the extraction of model parameters for device structures subject to the influence of penetrating radiation (as a result of a full-scale or computer experiment). By using the UTMOST4 module of Silvaco software package JFET, the model parameters were extracted under normal conditions and under the influence of penetrating radiation for the most sensitive parameters (VT0, LDEL, WDEL, RD, BETA, LAMBDA). The percentage error of the simulation using the extracted parameters set in comparison with the experimental data was no more than 7%.

5 Results

The simulation of the electrical characteristics of the JFET described by the developed model using the software package of the Cadence company was carried out and the coincidence of the simulation results of the electrical characteristics in the static mode with the results of the experimental data and the computer experiment data at the stage of the process and device simulation and the extraction was verified. Figure 3 shows the dependencies of the drain current on voltage at the drain for different values of neutron fluence with an energy of $E_N = 1{,}5$ MeV at a voltage at the gate of $V_G = 0$ V. The simulation results show deviations of no more than 5% from the values obtained during the extraction of the model parameters, which is explained by some assumptions in the construction of the approximation expressions for the dependence of the model parameters on the fluence and the energy of particles of penetrating radiation.

Figures 4 and 5 show the electrical characteristics of the device structure JFET exposed to just three types of penetrating radiation: neutrons with fluence $F_N = 2 \cdot 10^{15}$ cm^{-2} and energy $E_N = 1{,}5$ MeV, electrons with fluence $F_E = 10^{16}$ cm^{-2} and energy $E_E = 4$ MeV and protons with fluence $F_P = 6{,}6 \cdot 10^{11}$ cm^{-2} and energy $E_P = 2$ MeV.

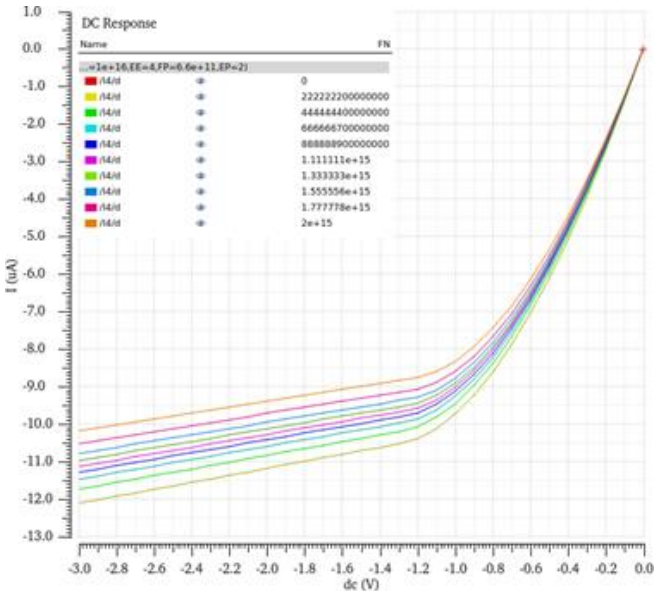

Fig. 3. Dependence $I_D(V_D)$ with neutron fluence variation with E_N = 1,5 MeV.

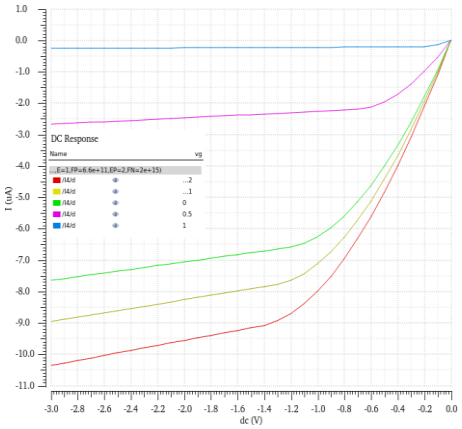

Fig. 4. Dependence I_D (V_D) when combined with the fluxes of neutrons, electrons and protons

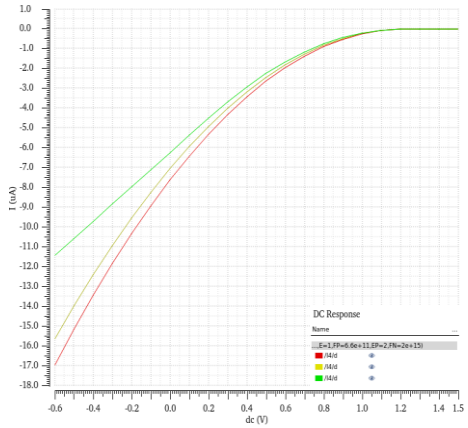

Fig. 5. Dependence I_D (V_D) when combined with the fluxes of neutrons, electrons and protons

For circuit simulation using the developed JFET model, a two-stage differential-input amplifier (Figure 4) is selected, which is subject to the influence of penetrating radiation. The main parameter of the amplifier is amplification factor (the noise level was not considered in the simulation). The supply voltage for the circuit is 9 V, the amplitude of input antiphase signal is 10 mV at a frequency of 1 kHz. The amplification factor for the considered circuit in normal conditions is 50.

Figure 5 shows the time diagrams (one half-period) under the influence of different neutron fluences with the energy of E_N = 1,5 MeV on all active circuit elements.

The simulation results show a significant change in the amplification factor (from a value of 50 to 60), despite the degradation changes in each of the transistors of the circuit. This effect can be explained by the features of circuit design, which ultimately demonstrates the possibility of optimizing the circuit to obtain the best performance.

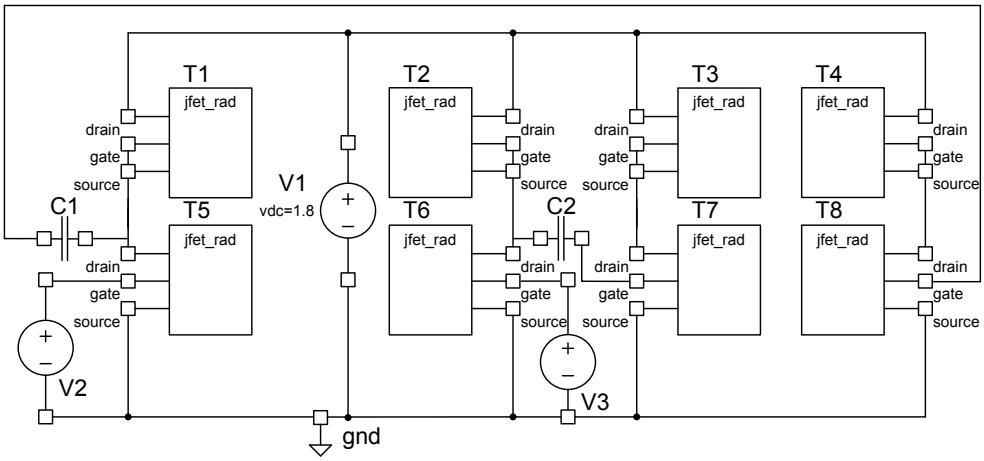

Fig. 4. Circuit diagram of a two-stage differential amplifier.

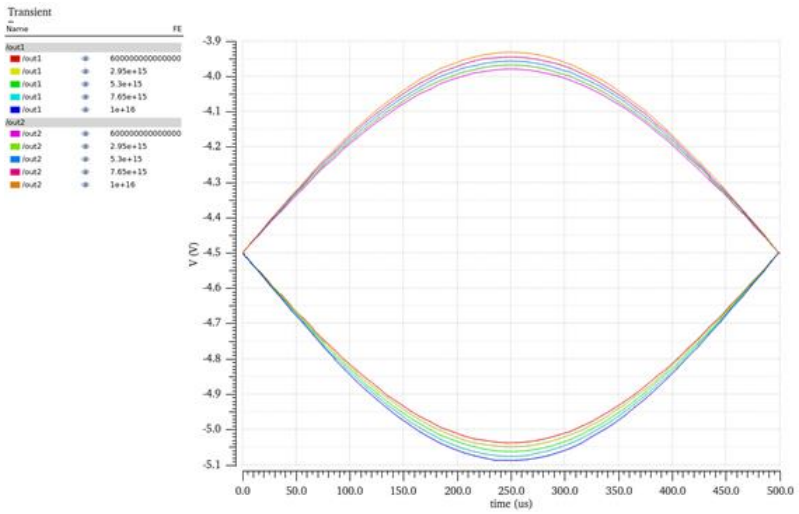

Fig. 5. Time diagram of a two-stage differential amplifier under normal conditions.

6 Conclusion

Integrated into Cadence software product compact model JFET with design standards of 1.5 microns implemented in the Verilog-A equipment description language, which allows one to take into account the influence of fluence and energy of electrons, protons and neutrons in circuit modeling (fluence to $F_E = 6 \cdot 10^{16}$ cm^{-2} with energy E_E from 3 to 5 MeV, $F_P = 6{,}6 \cdot 10^{11}$ cm^{-2} with energy E_P from 1 to 3 MeV, $F_N = 2 \cdot 10^{15}$ cm^{-2} with energy E_N from 1 to 2 MeV). An example of the application this model for predicting the behavior of semiconductor ICs special purposes under the conditions of exposure to radiation is given for a two-stage differential amplifier circuit.

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