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CODEC OF TWO DIMENSIONAL HAMMING CODES

Abstract
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INTRODUCTION

Advances in communication technology have revolutionized the way people exchange information across the world. The increasing reliance on digital communication systems has led to the development of sophisticated algorithms and techniques for error correction and data transmission. The need for efficient and reliable transmission of digital data has become a critical concern in fields such as telecommunications, data processing, and scientific research.

The transmission of digital data is inherently susceptible to errors, which can result in the loss or corruption of critical data. To address this issue, a variety of error correction techniques have been developed to ensure reliable transmission of digital data. Among these techniques, product codes have emerged as an effective means of error correction in digital communication systems.

The Hamming code is an information encoding method that uses bit sequences (0 or 1) to represent data. The advantage of Hamming code lies in its simplicity and reliability, as it can detect and correct errors. This is because the Hamming code uses a checksum calculated by an algorithm, which can detect any data corruption. The Hamming code is widely used in data communication, storage, and processing systems, and is valued for its simplicity, reliability, and efficiency.

Product codes are a type of error correction code that uses a combination of codes to correct errors in digital data. The use of product codes allows for highly efficient error correction, enabling digital communication systems to operate at high speeds and with high reliability. However, the implementation of product codes can be complex and resource-intensive, requiring sophisticated algorithms and high-performance computing systems.

The Hamming product code is an improvement over the Hamming code, achieving significantly higher error correction performance than conventional product codes with equivalent or slightly higher transmission overhead.

Field Programmable Gate Arrays (FPGAs) are widely used for the development of digital logic circuits due to their programmable nature and ability to implement complex designs with an elevated level of customization. FPGAs are used in a variety of applications such as signal processing, image and video processing, and cryptography.

In this work, a two-dimensional error correcting code is implemented on an FPGA for use in an on-chip or on-board system. Error correcting codes are used to detect and correct errors that may occur during data transmission or storage. The implementation of an error correcting code on an FPGA provides a fast and efficient way to handle errors in transmit and improve data integrity.

GENERAL DESCRIPTION OF WORK

Relevance of the subject

The work corresponds to paragraph 1 «Digital information and communication and interdisciplinary technologies, production based on them» of the State Program of innovative development of the Republic of Belarus for 2021–2025.

The work was carried out in the educational institution Belarusian State University of Informatics and Radioelectronics within the framework of research work 21-2033 "Processing, coding and transmission of information in network-centric systems".

The aim and tasks of the work

The aim of the work is to implement a 2D error correcting code on FPGA using hardware description language.

To achieve this aim, the following tasks were solved in the dissertation:

1 Analyze the background of the study

2 Analyze the 2D error correcting code and related works

3 Implement the 2D error correcting code on FPGA

4 Test the implementation’s functionality and performance

Personal contribution of the author

The content of the dissertation reflects the personal contribution of the author. In this work, a series of two-dimensional error correcting algorithms is implemented on an FPGA for use in an on-chip or on-board system provides a fast and efficient way to handle errors in transmit and improve data integrity.

Testing and implementation of results

The main provisions and results of the dissertation work were reported and discussed at: 59th scientific conference of postgraduates, undergraduates and students, (Minsk, April 18–22, 2023) and International scientific and technical seminar "Technologies of information transmission and processing" (Minsk, March – April 2022) and International scientific and technical seminar "Technologies of information transmission and processing" (Minsk, March - April 2023).

Author’s publications

According to the results of the research presented in the dissertation, 4 author’s works was published, including: 4 articles and abstracts in conference proceedings.

Structure and size of the work

The dissertation work consists of introduction, general description of the work, four chapters with conclusions for each chapter, conclusion, bibliography, eight appendixes.

The total amount of the thesis is 120 pages, of which 42 pages of text, 42 figures on 20 pages, 7 tables on 1 pages, a list of used bibliographic sources (25 titles on 2 pages), a list of the author's publications on the subject of the thesis (4 titles on 1 pages), graphic material on 12 pages.

Plagiarism

An examination of the dissertation «Title of the master's thesis» by Author's Full Name was carried out for the correctness of the use of borrowed materials using the network resource «Antiplagiat» (access address: https://antiplagiat.ru) in the on-line mode 20.05.2023. As a result of the verification, the correctness of the use of borrowed materials was established (the originality of the thesis is 99,62 %)

SUMMARY OF WORK

The introduction addresses the problems of two-dimensional error correcting code for on-chip or on-board system.

The general description of work shows the connection between the work and the priority areas of scientific research, the aim and tasks of the research, the personal contribution of the applicant for a scientific degree, the approbation of the dissertation results.

In the first chapter, we explore the background of the study, covering various aspects such as communication channels, on-board and on-chip communication methods, noises in the communication channel, error correction codes, and field programmable gate arrays. The chapter concludes by summarizing the key findings.

In the second chapter, we delve into the topic of 2D error correcting codes. We introduce the concept, discuss how to construct a 2D error correcting code, specifically focusing on the Hamming product code. We also explore different decode algorithms used in the study and examine existing implementations of the Hamming product code. The chapter concludes with a concise summary. Figure 1 shows the schematic of Hamming product code used in this work.

The third chapter focuses on the implementation of error correcting codes on FPGA (Field Programmable Gate Arrays). We outline the system structure, the tools and development environment used, and optimizations made on the decode algorithms. Furthermore, we provide detailed hardware design information, discuss different decode algorithm designs, and present the results of testing, simulation, and

RTL view. Finally, the chapter concludes by analyzing the performance and resource usage of the implemented system.

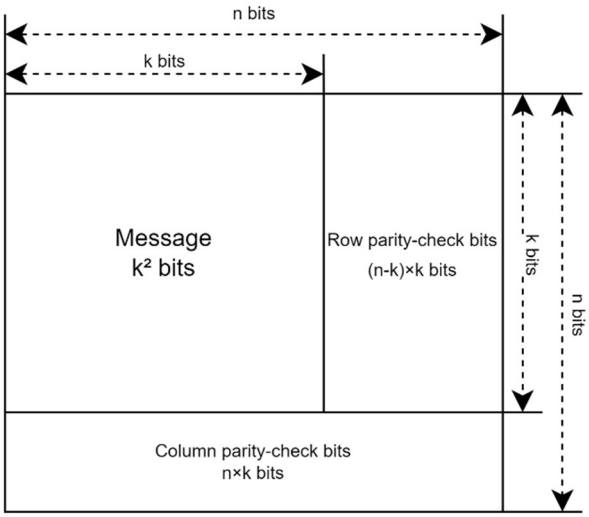

Figure 1 – Schematic of code used in this work

The device structure described in chapter 3 is shown in Figure 2, the design is mainly based on the message transmission direction and is divided into two main functional parts: transmitting and receiving. Implementing the code for the part of the virtual line is the main goal of this project.

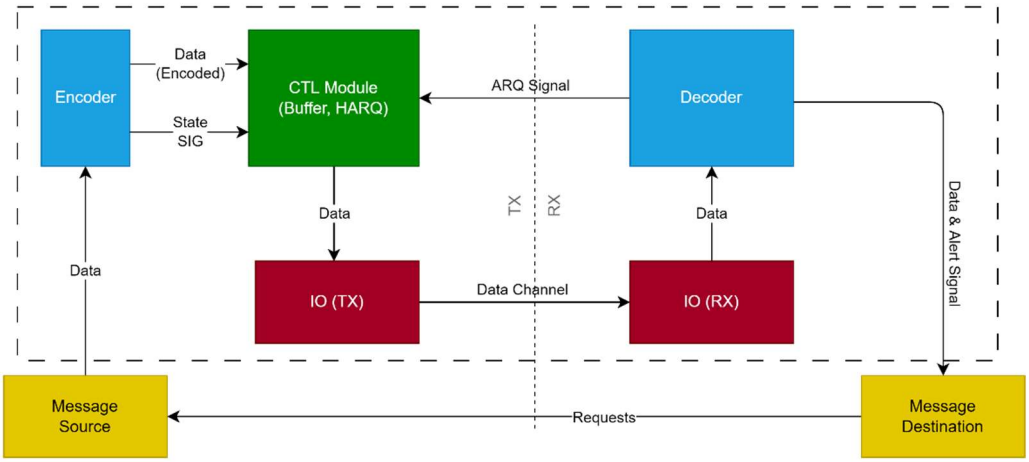

Figure 2 – System architecture overview

In the fourth chapter, we present a distributed testing system designed for large-scale tests. We describe the system architecture, discuss the deployment process, and outline the testing workflow. Additionally, we introduce a monitoring dashboard for

effective monitoring of the system. The chapter concludes with a brief summary of the findings in Chapter 4.

CONCLUSION

After an in-depth study of communication channels, on-board and on-chip communication methods, noises in communication channels, error correction codes, and field programmable gate arrays, this study focused on the implementation of 2D error-correcting codes on FPGA.

In the second chapter, we provided an introduction to 2D error-correcting codes and their properties, advantages, and how to construct and encode them. We also discussed the Hamming product code and decode algorithms used in the study.

The third chapter focused on the implementation of 2D error-correcting codes on FPGA. We provided an overview of the system structure, tools, and development environment used in the study. We also discussed the optimizations made to the decode algorithms, including matrix operations and loops. We delved into the hardware design details, including the encoder design, decoder frame design, and the MXIO library. We also discussed the decode algorithm to hardware designs, which included Bao's algorithm revision 3, standard Hamming product code, and Ren's extended Hamming product code. We evaluated the performance and resource usage of the system, using metrics such as resource usage and calculation of evaluating performance. Finally, we discussed the testing done on the system.

In the fourth chapter, we discussed a distributed testing system for large scale tests. We provided an overview of the system architecture and the deployment of the system. We also discussed the testing workflow and monitoring dashboard used in the study.

This study has shown that implementing 2D error-correcting codes on FPGA is a viable solution for improving communication channels. The optimizations made to the decode algorithms, hardware design details, and the use of the MXIO library have shown to improve the performance and resource usage of the system significantly. Additionally, the testing system provided a scalable solution for large scale testing, which can be useful in real-world applications.

In conclusion, this study has demonstrated the viability of implementing 2D error-correcting codes on FPGA to improve communication channels. The results have shown that the system can significantly improve performance with low resource usage while providing a scalable solution for large scale usage. Future research could focus on further optimizations and exploring other error-correcting codes that can be implemented on FPGA.

LIST OF AUTHOR'S PUBLICATIONS

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